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Time-to-Digit Converter Based on Radiation-Tolerant FPGA

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Time-to-Digit Converter (TDC)

is a coarse counter & **interpolator** (vernier)

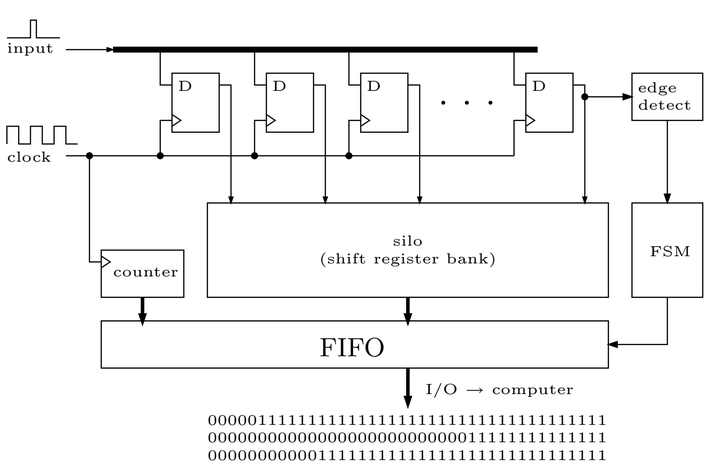
$$t = n_c T_0 + t_v, n_c \in N, t_v \in \langle 0, T_0)$$

Objectives

- $<$ 50 $\mathrm{ps_{RMS}}$, $>$ 10 ksps for single-photon applications (laser ranging, time transfer)
- radiation-tolerant, space-qualified components solution

Our design

- passive tapped delay line
- all-digital, 1-bit sampling by flip-flops
- whole bit-vector recorded for detailed analysis
- stochastic (re-)calibration



Pros/Cons

⊕ pure digital (standard FPGA/CMOS)
⊕ scalable
• more ICs/larger IC ... between $1/N$ to $1/\sqrt{N}$
⊕ single principal component
• radiation-tolerant FPGA for space appliactions
⊖ better performing circuits exist ($<$ 1 $\mathrm{ps_{RMS}}$)

Similar solutions

- [3]
  active delay line
- BOUNCE [4]
  does not preserve whole bit vector (information loss)
  use of manual, deterministic calibration
  slightly worse results in faster FPGA

Other remarkable solutions

- N-PET [1]
  requires SAW filter & ADC
- "Riga" event timer (3 $\mathrm{ps_{RMS}}$?)
  probably integrator & ADC
- ACAM company's integrated circuit
  probably ASIC, similar performance

References

[1] P. Panek, I. Prochazka. Time interval measurement device based on SAW filter excitation ... IEEE Review of Scientific Instruments, 2004

[2] W. Becker. Advanced Time-Correlated Single Photon Counting Techniques: Springer-Verlag, 2005

[3] Y. Zhang, P. Huang, R. Zhu. Upgrading of integration of time to digit converter on a single FPGA. Proc. 15th Int. Laser Ranging Workshop

[4] R. Salomon, R. Joost. BOUNCE: A New High-Resolution Time-Interval Measurement Architecture. IEEE Embedded Systems Letters, 2009

Stochastic calibration

Random pulse source & histogram → non-linearity estimation (mentioned briefly in [2])

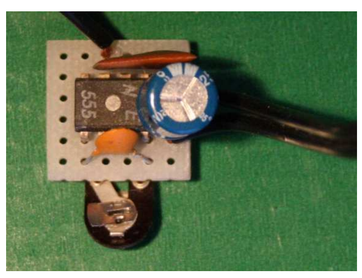
Non-linearity compensation uncertainty after N random events (negligible jitter assumed):

$$\sigma_t = \frac{T_0}{2\sqrt{N}}$$

Note Large jitter would cause biased estimates; investigation of jitter observability from the bit vector is in progress...

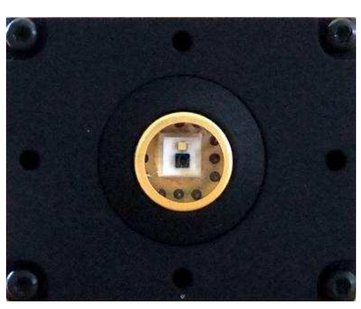
Random sources

RC oscillator (NE555); high phase-noise $t \sim \mathcal{U}(0, T_0)$



Single-photon avalanche diode (SPAD)

- non-gated: $t \sim \mathcal{U}(0, T_0)$
- gated coherently with clock → exponential-like pdf



Benefits

- alternative to deterministic calibration
- *in-situ* (on-board) stability check
- long-term recalibration (drift, aging)

Performance

Two main uncertainty factors:

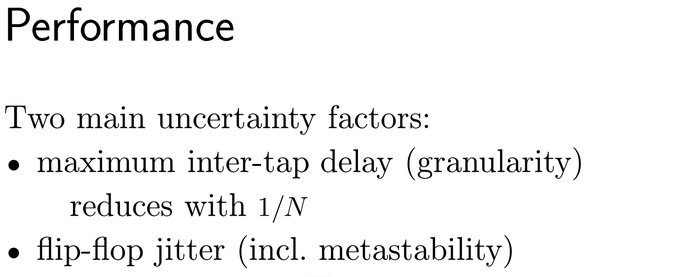
- maximum inter-tap delay (granularity)
  reduces with $1/N$
- flip-flop jitter (incl. metastability)
  reduces with $1/\sqrt{N}$

Current limit: **inter-tap delay**

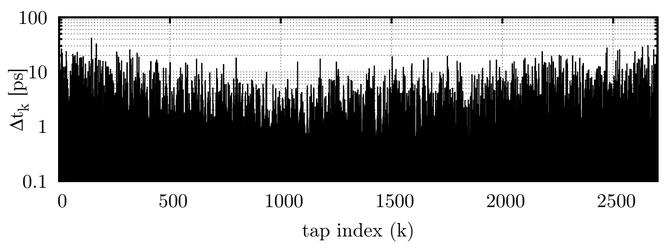
- → worst-case deterministic error $\Delta t_{max} = \frac{1}{2}\min_k \Delta t_k$
- → RMS of deterministic error ($t \sim \mathcal{U}(0, T_0)$ assumed): $\Delta t^2_{RMS} = \frac{1}{12T_0}\sum_{k=1}^{N} \Delta t_k^3$

Topology (FPGA floor-plan) impact on inter-tap delay

Design #1, 320 taps, Δt_{max} = 87.6 ps, Δt_{RMS} = 24.8 ps



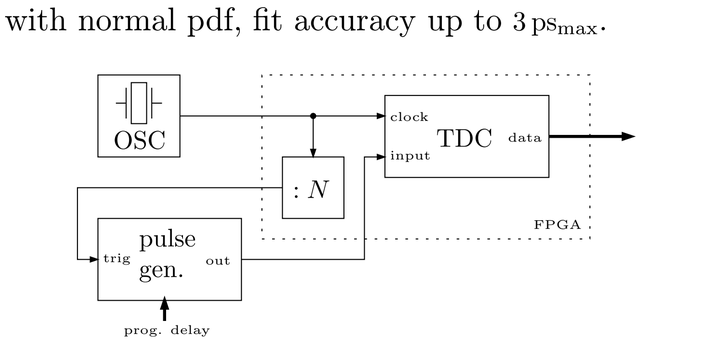
Design #2, 2700 taps, Δt_{max} = 20.7 ps, Δt_{RMS} = 3.03 ps

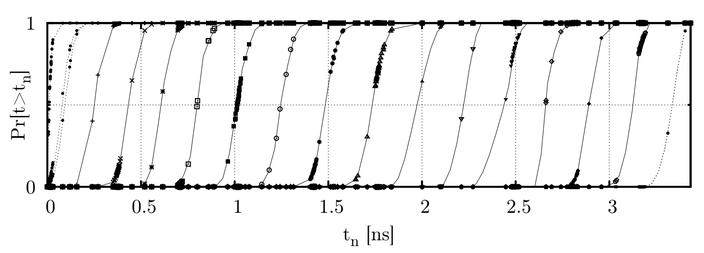


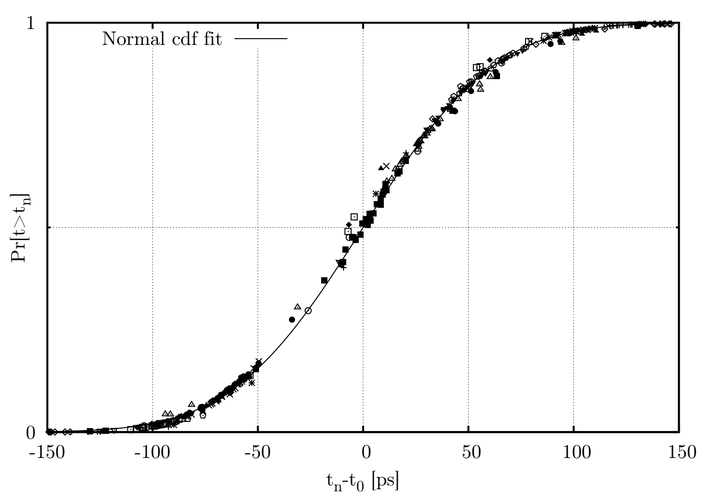
Results

Signal chain with noise

Measurement chain: 49 $\mathrm{ps_{RMS}}$ jitter, caused by on-chip PLL and pulse delay generator. Jitter fitted with normal pdf, fit accuracy up to 3 $\mathrm{ps_{max}}$.

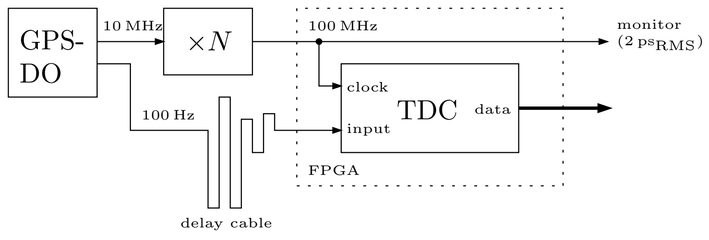


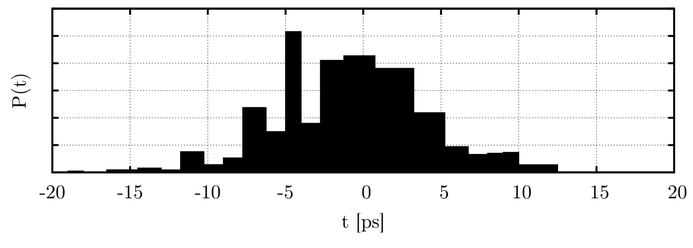




Stable signal

- GPS-DO clock & pulse source
- 10 → 100 MHz clock from coherent multiplier
- one-point (cable delay) measurement





- **worst-case deterministic error (Δt_{max}) 20.7 ps**
- **RMS deterministic error (Δt_{RMS}): 3.03 ps**
- **random jitter (RMS σ): 4.93 ps**

Future work

- measure temperature & **long-term** stability
- evaluate impact of flip-flops **metastability**
- try to **self-estimate jitter** from whole bit vector data to improve histogram calibration (underdetermined task?)