MF 624

MULTIFUNCTION I/O CARD

USER'S MANUAL

HUMUSOFT®

Printed in Czech Republic

Table of Contents

1. Introduction

1.1. General Description

The MF 624 multifunction I/O card is designed for the need of connecting PC compatible computers to real world signals. The MF 624 contains 8 channel fast 14 bit A/D converter with simultaneous sample/hold circuit, 8 independent 14 bit D/A converters, 8 bit digital input port and 8 bit digital output port, 4 quadrature encoder inputs with single-ended or differential interface and 5 timers/counters. The card is designed for standard data acquisition and control applications and optimized for use with Real Time Toolbox for Simulink®. MF 624 features fully 32 bit architecture for fast throughput.

1.2. Features List

The MF 624 offers following features:

- 32-bit architecture
- 14 bit A/D converter with simultaneous sample & hold circuit
- Conversion time 1.6 µs for single channel or 3.7 µs for 8 channels
- 8 channel single ended fault protected input multiplexer
- Input range ±10V
- Internal clock & voltage reference
- 8 D/A converters with 14 bit resolution and ±10V output range
- 4 quadrature encoder inputs with single-ended or differential interface
- Software selectable digital input noise filter (0.3 µs)

- Quadrature input frequency up to 2.5 MHz
- Software selectable index pulse operation
- 4 channel 32-bit timer/counter with 20 ns resolution
- 8 bit TTL compatible digital input port
- 8 bit TTL compatible digital output port
- Interrupt
- Requires one PCI 2.3 slot and optional second slot for second connector
- Can be used in 5V or 3.3V slot
- Power consumption 500 mA@+5V, 150 mA@+12V, 150 mA@-12V
- Operating temperature 0°C to +70°C

1.3. Specifications

1.3.1. A/D Converter

Resolution:	14 bits
Number of channels:	8 single ended
Sample/hold circuit:	simultaneous sampling of all channels
Conversion time:	1.6 µs single channel
	1.9 µs 2 channels
	2.5 µs 4 channels
	3.7 µs 8 channels
FIFO:	8 entries/one conversion cycle
Input ranges:	±10V
Input protection:	±18V
Input impedance:	> 10^{10} Ohm

1.3.2. D/A Converter

Resolution:	14 bit
Number of channels:	8
Settling time:	max. 31 µs (full scale swing, 1/2 LSB)
Slew Rate:	10 V/µs
Output current:	min. ±10 mA
Short circuit current:	±15 mA
DC output impedance:	max. 0.5 Ohm
Load capacitance:	max. 50 pF
Differential nonlinearity:	±1 LSB

1.3.3. Digital Inputs

Number of bits:	8
Input signal levels:	TTL
Logic 0:	0.8 V max.
Logic 1:	2.0 V min.

1.3.4. Digital Outputs

Number of bits:	8
Output signal levels:	TTL
Logic 0:	0.5 V max. @ 24 mA (sink)
Logic 1:	2.0 V min. @ 15 mA (source)

1.3.5. Quadrature Encoder Inputs

Number of axes:	4 independent
Resolution:	32 bits

Counter modes:	quadrature X4 or up/down counter
Index input:	programmable
Inputs:	differential with Schmitt triggers
Input noise filter:	digital, programmable (0.3 µs)
Input frequency:	max. 2.5 MHz

1.3.6. Counters/Timers

Counter chip:	custom
Number of channels:	5, 4 of them available on I/O connector, one used for A/D triggering and interrupt
Resolution:	32 bits
Clock frequency:	50 MHZ
Counter modes:	up, down, binary
Triggering:	software, external
Clock source:	internal, prescalers, external
Inputs:	TTL, Schmitt triggers
Outputs:	TTL

2. Installation

2.1. Board Installation

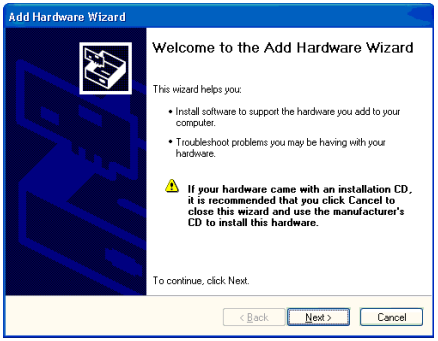
MF 624 has no switches or jumpers and you can install it in any free PCI expansion slot of your computer. Follow the steps outlined below:

- Turn off the power of the computer system and unplug the power cord.
- Disconnect all cables connected to the computer system.
- Using a screwdriver, remove the cover-mounting screws. These screws are at the rear side of the PC.
- Remove the computer system's cover.
- Find an empty expansion slot in your computer for MF 624 card. If the slot still has the metal expansion-slot cover attached, remove the cover with a screwdriver. Save the screw to install the MF 624.
- Hold the MF 624 firmly at the top of the board, and press the gold edge connector into an empty PCI expansion slot.
- Using a screwdriver, screw the retaining bracket tightly against the rear plate of the computer system.
- In case of using also quadrature encoder inputs or timer/counters install also the aditional connector with metal slot cover to the neighbouring slot. Otherwise you can disconnect the aditional connector from the board and save it for future use.
- Replace the cover of the computer, and plug in the power cord.
- Reconnect all cables that were previously attached to the rear of the computer.

2.2. Driver Installation

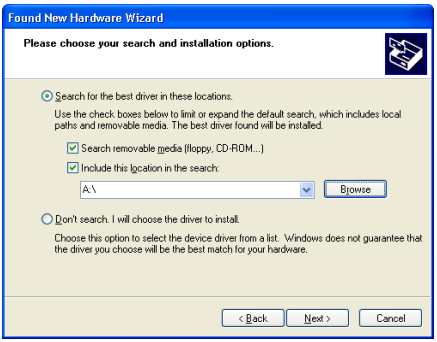
Once you have installed MF 624 to PCI slot you can install Windows driver. Follow the steps outlined below:

Turn on the computer, boot Microsoft Windows. MF 624 is detected by system automatically. In Add Hardware Wizzard window click Next.



Insert installation floppy into drive a. In Found New Hardware Wizzard select Install the software automatically and click Next.

When prompted for driver location type a:\ and click Next. Click Finish to complete installation.



3. Programming Guide

3.1. Register Map

MF 624 uses PCI Vendor ID 0x186C and Device ID 0x0624. Registers of MF 624 card are located in 3 memory mapped regions:

Region	**Function**	**Size (bytes)**	**Width (bits)**
BADR0 (memory mapped)	PCI chipset, interrupts, status bits, special functions	32	32
BADR1 (memory mapped)	A/D, D/A, digital I/O	128	16/32
BADR2 (memory mapped)	Counter/timer chip	128	32

Table 1. Base Address Regions

PCI chipset (PCI 9030) and counter/timer chip are located in 32-bit regions and should be accessed by 32-bit instructions. BADR1 containing analog I/O has 16-bit architecture and registers are naturally 16-bit wide, but 32-bit access to this area is allowed as well under certain conditions. 32-bit access is broken by PCI chipset into two 16-bit cycles on the MF 624 internal bus. This allows increasing throughput by accessing two consecutive internal 16-bit registers by single PCI cycle. Therefore two D/A channels can be written or two A/D channels can be read at once which increases speed of data transfers almost twice. Do not use 32-bit access to other registers than ADDATA and DA0 - DA7.

Address	Read	Write
BADR0+0x4C	**INTCSR**	**INTCSR**
BADR0+0x54	**GPIOC**	**GPIOC**

Table 2. BADR0 Memory Map

Address	Read	Write
BADR1+0x00	**ADDATA** - A/D data	**ADCTRL** - A/D control
BADR1+0x02	**ADDATA** - A/D data mirror	
BADR1+0x04	**ADDATA** - A/D data mirror	
BADR1+0x06	**ADDATA** - A/D data mirror	
BADR1+0x08	**ADDATA** - A/D data mirror	
BADR1+0x0A	**ADDATA** - A/D data mirror	
BADR1+0x0C	**ADDATA** - A/D data mirror	
BADR1+0x0E	**ADDATA** - A/D data mirror	
BADR1+0x10	**DIN** - Digital input	**DOUT** - Digital output
BADR1+0x20	**ADSTART** - A/D SW trigger	**DA0** - D/A 0 data
BADR1+0x22		**DA1** - D/A 1 data
BADR1+0x24		**DA2** - D/A 2 data
BADR1+0x26		**DA3** - D/A 3 data
BADR1+0x28		**DA4** - D/A 4 data
BADR1+0x2A		**DA5** - D/A 5 data
BADR1+0x2C		**DA6** - D/A 6 data
BADR1+0x2E		**DA7** - D/A 7 data

Table 3. BADR1 Memory Map

Address	Read	Write
BADR2+0x00	**CTR0STATUS**	**CTR0MODE**
BADR2+0x04	**CTR0**	**CTR0A**
BADR2+0x08		**CTR0B**
BADR2+0x10	**CTR1STATUS**	**CTR1MODE**
BADR2+0x14	**CTR1**	**CTR1A**
BADR2+0x18		**CTR1B**
BADR2+0x20	**CTR2STATUS**	**CTR2MODE**
BADR2+0x24	**CTR2**	**CTR2A**
BADR2+0x28		**CTR2B**
BADR2+0x30	**CTR3STATUS**	**CTR3MODE**
BADR2+0x34	**CTR3**	**CTR3A**
BADR2+0x38		**CTR3B**
BADR2+0x40	**CTR4STATUS**	**CTR4MODE**
BADR2+0x44	**CTR4**	**CTR4A**
BADR2+0x48		
BADR2+0x60		**CTRXCTRL**
BADR2+0x6C	**IRCSTATUS**	**IRCCTRL**
BADR2+0x70	**IRC0**	
BADR2+0x74	**IRC1**	
BADR2+0x78	**IRC2**	
BADR2+0x7C	**IRC3**	

Table 4. BADR2 Memory Map

3.2. Register Description

INTCSR **BADR0+0x4C** **Interrupt Control/Status** **R/W**

Bit	Description	Default
0	**ADINT Enable**. 1 enables A/D interrupt, 0 disables A/D interrupt.	0
1	**ADINT Polarity**. 1 active high, 0 active low. Connected to **EOLC** of A/D converter, should be set to active low for normal operation.	0
2	**ADINT Status**. 1 indicates interrupt active, 0 indicates interrupt not active.	0
3	**CTR4INT Enable**. 1 enables counter 4 (or external trigger) interrupt, 0 disables counter 4 interrupt.	0
4	**CTR4INT Polarity**. 1 active high, 0 active low. Connected to counter 4 output (or external trigger input).	0
5	**CTR4INT Status**. 1 indicates interrupt active, 0 indicates interrupt not active.	0
6	**PCI Interrupt Enable**. 1 enables PCI interrupt.	0
7	**Software Interrupt**. 1 generates PCI interrupt (INTA#) if PCI Interrupt Enable bit is set (bit [6]=1).	0
8	**ADINT Select Enable**. 1 indicates edge triggered, 0 indicates level triggered interrupt. ***Note:*** *Operates only in High-Polarity mode (bit [1]=1)*	0
9	**CTR4INT Select Enable**. 1 indicates edge triggered, 0 indicates level triggered interrupt. Note: Operates only in High-Polarity mode (bit [4]=1)	0
10	**ADINT Clear**. Writing 1 to this bit clears ADINT in edge mode.	0
11	**CTR4INT Clear**. Writing 1 to this bit clears CTR4INT in edge mode.	0
31:12	Reserved	0x000300

Table 5. INTCSR - Interrupt Control/Status Register Format

GPIOC **BADR0+0x54** **Genaral Purpose I/O Control** **R/W**

Bit	Description	Default
16:0	Reserved.	0x006C0
17	**EOLC**. Reads EOLC (end of last conversion) bit of A/D converter. Active low, 0 when all channels converted, 1 during A/D conversion.	0
21:18	Reserved.	0x10
23	**LDAC**. Load D/A converters, active low. Writing 0 makes A/D latches transparent, 1 holds D/A outputs. Can be used for simultaneous update of analog outputs.	0
25:24	Reserved.	10
26	**DACEN**. 1 enables D/A outputs. 0 forces 0V to all D/A outputs.	0
31:27	Reserved.	0

Table 6. GPIOC - General Purpose I/O Control Register Format

ADCTRL **BADR1+0x00** **A/D Control** **W**

Bit	Description	Default
0	**CH0 select**. 1 enables chanel 0 in channel scan list.	0
1	**CH1 select**. 1 enables chanel 1 in channel scan list.	0
2	**CH2 select**. 1 enables chanel 2 in channel scan list.	0
3	**CH3 select**. 1 enables chanel 3 in channel scan list.	0
4	**CH4 select**. 1 enables chanel 4 in channel scan list.	0
5	**CH5 select**. 1 enables chanel 5 in channel scan list.	0
6	**CH6 select**. 1 enables chanel 6 in channel scan list.	0
7	**CH7 select**. 1 enables chanel 7 in channel scan list.	0
15:8	Reserved.	0x00

Table 7. ADCTRL - A/D Control Register Format

ADDATA BADR1+0x00 A/D Data R

Bit	Description	Default
13:0	**A/D Data.** Reads data from A/D. Data is valid after EOLC bit in GPIOC goes low. Data from channels selected in ADCTRL register are available in FIFO, lower number channels first.	N/A
15:14	Reserved	N/A

Table 8. ADDATA - A/D DATA Register Format

Note: *ADDATA register has 7 mirror registers located from BADR1+0x02 to BADR1+0x0E. This arrangement remaps FIFO to linear address space and allows reading consecutive values from A/D FIFO by 32-bit instructions.*

DIN BADR1+0x10 Digital Input R

Bit	Description	Default
7:0	**Digital input 7:0.** Reads digital input port.	1
15:8	Reserved	N/A

Table 9. DIN - Digital Input Register Format

DOUT BADR1+0x10 Digital Output W

Bit	Description	Default
7:0	**Digital output 7:0.** Writes to digital output port.	0
15:8	Reserved	N/A

Table 10. DOUT - Digital Output Register Format

ADSTART BADR1+0x20 A/D Conversion Start R

Bit	Description	Default
15:0	**A/D Conversion Start.** Reading this register triggers A/D conversion for all channels selected in ADCTRL.	N/A

Table 11. ADSTART - A/D Conversion Start Register Format

DA0	**BADR1+0x20**	**D/A Converter 0**	**W**
DA1	**BADR1+0x22**	**D/A Converter 1**	**W**
DA2	**BADR1+0x24**	**D/A Converter 2**	**W**
DA3	**BADR1+0x26**	**D/A Converter 3**	**W**
DA4	**BADR1+0x28**	**D/A Converter 4**	**W**
DA5	**BADR1+0x2A**	**D/A Converter 5**	**W**
DA6	**BADR1+0x2C**	**D/A Converter 6**	**W**
DA7	**BADR1+0x2E**	**D/A Converter 7**	**W**

Bit	Description	Default
13:0	**DAx**. D/A converter channel n data.	0x3FFF
15:14	Reserved.	N/A

Table 12. DAx - D/A Converter Data Register Format

Note: *D/A converter outputs are updated only if LDAC bit in GPIOC registrer is set low (bit [23] at BADR0+0x54 =0). Otherwise D/A outputs are keeping old values and data written to DAn registers are kept until LDAC goes low. LDAC bit can be used for simultaneous update of D/A outputs.*

CTR0STATUS	**BADR2+0x00**	**Counter 0 Status**	**R**
CTR1STATUS	**BADR2+0x10**	**Counter 1 Status**	**R**
CTR2STATUS	**BADR2+0x20**	**Counter 2 Status**	**R**
CTR3STATUS	**BADR2+0x30**	**Counter 3 Status**	**R**
CTR4STATUS	**BADR2+0x40**	**Counter 4 Status**	**R**

Bit	Description	Default
0	**Counter Running**. 1 if counter is running, 0 if stopped.	0
1	**Counter Output**. Reads counter toggle output.	0
31:2	Reserved.	N/A

Table 13. CTRxSTATUS - Counter Status Register Format

CTR0MODE	**BADR2+0x00**	**Counter 0 Mode**	**W**
CTR1MODE	**BADR2+0x10**	**Counter 1 Mode**	**W**
CTR2MODE	**BADR2+0x20**	**Counter 2 Mode**	**W**
CTR3MODE	**BADR2+0x30**	**Counter 3 Mode**	**W**
CTR4MODE	**BADR2+0x40**	**Counter 4 Mode**	**W**

Bit	Description	Default
0	**Count Direction**. 1 counts up, 0 counts down.	0
1	**Repetition**. If 0, counter stops after terminal count. If 1, counter reloads after terminal count and starts new cycle.	0
2	**Load Toggle**. If 0, counter always reloads from register A on terminal count. If 1, counter reloads alternately from A register or from B register depending on output toggle status.	0
3	**Output Toggle**. If 0, counter output pin is connected to terminal count. If 1 counter output is connected to output toggle which is inverted on every terminal count.	0
5:4	**Output Control**. Controls output value and polarity. 00: direct output 01: inverted output 10: force output low 11: force output high	10
7:6	**Trigger source**. Controls counter hardware trigger source. 00: trigger disabled 01: trigger by counter input (TxIN) 10: trigger by counter n-1 output 11: trigger by counter n+1 output	0
9:8	**Trigger type**. Controls counter hardware trigger edge. 00: trigger disabled 01: trigger by rising edge of trigger signal 10: trigger by falling edge of trigger signal 11: trigger by either edge of trigger signal	0
10	**Retrigger**. If 0, retrigger is disabled and counter can be triggered only when stopped. If 1, counter can be retriggered when running.	0

12:11	**Gate source**. Controls counter hardware gate source. 00: gate set high 01: counter gated by counter input (TxIN) 10: counter gated by counter n-1 output 11: counter gated by counter n+1 output	0
13	**Gate polarity**. Selects value of gate input which disables counting. If set to 0, low level of gate signal disables counting. If set to 1, high level of gate signal disables counting.	0
17:14	**Clock source**. Selects counter clock source. 0000: 50 MHz internal clock 0001: 10 MHz internal clock 0010: 1 MHz internal clock 0011: 100 kHz internal clock 0100: reserved 0101: counter input (TxIN) rising edge 0110: counter input (TxIN) falling edge 0111: counter input (TxIN) either edge 1000: reserved 1001: counter n-1 output rising edge 1010: counter n-1 output falling edge 1011: counter n-1 output either edge 1100: reserved 1101: counter n+1 output rising edge 1110: counter n+1 output falling edge 1111: counter n+1 output either edge	0
29:18	Reserved	0
30	**ADTRIGSRC**. A/D trigger source. 0 triggers by falling edge of counter 4 output. 1 triggers by falling edge of external trigger input. Implemented in CTR4MODE register only.	0
31	**CTR4INTSRC**. Interrupt signal source. 0 interrupts by falling edge of counter 4 output. 1 interrupts by falling edge of external trigger input. Implemented in CTR4MODE register only.	0

Table 14. CTRxMODE - Counter Mode Register Format

CTR0	**BADR2+0x04**	**Counter 0 Data**	**R**
CTR1	**BADR2+0x14**	**Counter 1 Data**	**R**
CTR2	**BADR2+0x24**	**Counter 2 Data**	**R**
CTR3	**BADR2+0x34**	**Counter 3 Data**	**R**
CTR4	**BADR2+0x44**	**Counter 4 Data**	**R**

Bit	Description	Default
31:0	**Counter Data**. Reads current contents of counter.	0

Table 15. CTRx - Counter Data Register Format

CTR0A	**BADR2+0x04**	**Counter 0 Load A**	**W**
CTR1A	**BADR2+0x14**	**Counter 1 Load A**	**W**
CTR2A	**BADR2+0x24**	**Counter 2 Load A**	**W**
CTR3A	**BADR2+0x34**	**Counter 3 Load A**	**W**
CTR4A	**BADR2+0x44**	**Counter 4 Load A**	**W**

Bit	Description	Default
31:0	**Counter Load A**. Counter load register A	0

Table 16. CTRxA - Counter Load A Register Format

CTR0B	**BADR2+0x08**	**Counter 0 Load B**	**W**
CTR1B	**BADR2+0x18**	**Counter 1 Load B**	**W**
CTR2B	**BADR2+0x28**	**Counter 2 Load B**	**W**
CTR3B	**BADR2+0x38**	**Counter 3 Load B**	**W**

Bit	Description	Default
31:0	**Counter Load B**. Counter load register B	0

Table 17. CTRxB - Counter Load B Register Format

Note: *Counter 4 does not have Load B register and is always being loaded from Load A register.*

CTRXCTRL BADR2+0x60 Counter Conrol Register W

Bit	Description	Default
0	**CTR0START**. Writing 1 starts counter 0.	0
1	**CTR0STOP**. Writing 1 stops counter 0.	0
2	**CTR0LOAD**. Writing 1 loads counter 0 from Load A or Load B register.	0
3	**CTR0RESET**. Writing 1 resets counter 0.	0
4	**CTR0TSET**. Writing 1 sets counter 0 output toggle register.	0
5	**CTR0TRESET**. Writing 1 resets counter 0 output toggle register.	0
6	**CTR1START**. Writing 1 starts counter 1.	0
7	**CTR1STOP**. Writing 1 stops counter 1.	0
8	**CTR1LOAD**. Writing 1 loads counter 1 from Load A or Load B register.	0
9	**CTR1RESET**. Writing 1 resets counter 1.	0
10	**CTR1TSET**. Writing 1 sets counter 1 output toggle register.	0
11	**CTR1TRESET**. Writing 1 resets counter 1 output toggle register.	0
12	**CTR2START**. Writing 1 starts counter 2.	0
13	**CTR2STOP**. Writing 1 stops counter 2.	0
14	**CTR2LOAD**. Writing 1 loads counter 2 from Load A or Load B register.	0
15	**CTR2RESET**. Writing 1 resets counter 2.	0
16	**CTR2TSET**. Writing 1 sets counter 2 output toggle register.	0
17	**CTR2TRESET**. Writing 1 resets counter 2 output toggle register.	0
18	**CTR3START**. Writing 1 starts counter 3.	0
19	**CTR3STOP**. Writing 1 stops counter 3.	0
20	**CTR3LOAD**. Writing 1 loads counter 3 from Load A or Load B register.	0
21	**CTR3RESET**. Writing 1 resets counter 3.	0

22	**CTR3TSET**. Writing 1 sets counter 3 output toggle register.	0
23	**CTR3TRESET**. Writing 1 resets counter 3 output toggle register.	0
24	**CTR4START**. Writing 1 starts counter 4.	0
25	**CTR4STOP**. Writing 1 stops counter 4.	0
26	**CTR4LOAD**. Writing 1 loads counter 4 from Load A or Load B register.	0
27	**CTR4RESET**. Writing 1 resets counter 4.	0
28	**CTR4TSET**. Writing 1 sets counter 4 output toggle register.	0
29	**CTR4TRESET**. Writing 1 resets counter 4 output toggle register.	0
31:30	Reserved.	0

Table 18. CTRXCTRL - Common Counter Control Register Format

Note: *Bits 29:0 are active by writing 1. Writing 0 to these bits is not necessary and has no action asigned.*

IRCCTRL BADR2+0x6C IRC Conrol Register W

Bit	Description	Default
1:0	**IRC0MODE**. Selects IRC0 counter operation. 00: IRC, 4 edge detection 01: bidirectional counter, rising edge 10: bidirectional counter, falling edge 11: bidirectional counter, either edge	0
3:2	**IRC0COUNT**. IRC0 count control. 00: IRC0 count enabled 01: IRC0 count disabled 10: IRC0 count enabled if I0 input is 0 11: IRC0 count enabled if I0 input is 1	0
6:4	**IRC0RESET**. IRC0 reset control. 000: IRC0 reset disabled 001: IRC0 reset 010: IRC0 reset if I0 is 0 011: IRC0 reset if I0 is 1 100: IRC0 reset by rising edge of I0 101: IRC0 reset by falling edge of I0 110: IRC0 reset by either edge of I0 111: Reserved	0
7	**IRC0FILTER**. IRC0 digital filter control. 1 enables digital filter on IRC0 inputs. 0 disables filtering.	0
9:8	**IRC1MODE**. Selects IRC1 counter operation. See IRC0MODE	0
11:10	**IRC1COUNT**. IRC1 count control. See IRC0COUNT	0
14:12	**IRC1RESET**. IRC1 reset control. See IRC0RESET	0
15	**IRC1FILTER**. IRC1 digital filter control. 1 enables digital filter on IRC1 inputs. 0 disables filtering.	0
17:16	**IRC2MODE**. Selects IRC2 counter operation. See IRC0MODE	0
19:18	**IRC2COUNT**. IRC2 count control. See IRC0COUNT	0
22:20	**IRC2RESET**. IRC2 reset control. See IRC0RESET	0

23	**IRC2FILTER**. IRC2 digital filter control. 1 enables digital filter on IRC2 inputs. 0 disables filtering.	0
25:24	**IRC3MODE**. Selects IRC3 counter operation. See IRC0MODE	0
27:26	**IRC3COUNT**. IRC3 count control. See IRC0COUNT	0
30:28	**IRC3RESET**. IRC3 reset control. See IRC0RESET	0
31	**IRC3FILTER**. IRC3 digital filter control. 1 enables digital filter on IRC3 inputs. 0 disables filtering.	0

Table 19. IRCCTRL - IRC Control Register Format

Note: *Digital filter on IRC inputs is a low-pass filter improving noise immunity. The filter also decreases maximum input frequency and signal changes shorter than 320 ns are ignored.*

IRCSTATUS BADR2+0x6C IRC Status Register R

Bit	Description	Default
0	**IRC0INDEX**. Reads I0 input.	1
7:1	**Reserved**.	N/A
8	**IRC1INDEX**. Reads I1 input.	1
15:9	**Reserved**.	N/A
16	**IRC2INDEX**. Reads I3 input.	1
23:17	**Reserved**.	N/A
24	**IRC3INDEX**. Reads I3 input.	1
31:25	**Reserved**.	N/A

Table 20. IRCSTATUS - IRC Status Register Format

IRC0	**BADR2+0x70**	**IRC0 Data Register**	**R**
IRC1	**BADR2+0x74**	**IRC1 Data Register**	
IRC2	**BADR2+0x78**	**IRC2 Data Register**	
IRC3	**BADR2+0x7C**	**IRC3 Data Register**	

Bit	Description	Default
31:0	**IRCx**. Reads data from IRC counter.	0

Table 21. IRCx - IRCx Data Register Format

3.3. A/D Converter

A/D converter is controlled through ADDATA, ADCTRL, ADSTART and GPIOC registers.

Before starting a conversion it is necessary to configure channels which will be converted by ADCTRL register. Each A/D channel has one bit in ADCTRL. Setting this bit includes the channel in conversion scan list. Conversion can be initiated by a read operation from ADSTART register, by timer/counter T4 or by external trigger. Once the conversion is started, selected channels are simultaneously sampled and converted. When the conversion of all selected channels is complete, EOLC (bit 17 in GPIOC register) is set low which means that converted data is available in output FIFO and can be read from ADDATA register. EOLC remains low until next conversion is started. Starting new conversion resets FIFO.

A/D conversion can be triggered also by timer 4 output or by external trigger input according to setting of ADTRIGSRC (bit 30 in CTRXCTRL register). These signals can also generate interrupt according to setting of INT2SRC (bit 31 in CTRXCTRL register).

A/D converter has fixed input range ±10V and uses two's complement binary coding. A/D converter zero offset can be adjusted by R23. A/D gain can be adjusted by R25.

Digital Value	Analog Voltage
0x3FFF	-0.0012 V
0x2000	-10.0000 V
0x1FFF	9.9988 V
0x0000	0.0000 V

Table 22. A/D Inputs Coding

3.4. D/A Converters

D/A converters are accessed through eight data input latch registers DA0 - DA7. D/A converter outputs are initially connected to ground until DACEN (bit 26 in GPIOC register) is set to 1. This bit can be used to disconnecting all analog outputs from D/A converters. Data from D/A input latch registers are passed to D/A converters only if LDAC (bit 23 in GPIOC register) is 0. If this bit is set to 1, data remains just in input latches without being written to D/A converters. Then if LDAC is set to 0, all D/A outputs are updated simultaneously from input latch registers.

Output voltage ranges of D/A converters are ±10V and straight binary coding is used. After power-on or hardware reset the output voltage is set to 0V. D/A converter positive range can be adjusted by R5 while negative range can be adjusted by R8.

Digital Value	Analog Voltage
0x3FFF	9.9988 V
0x2000	0.0000 V
0x1FFF	-0.0012 V
0x0000	-10.0000 V

Table 23. D/A Outputs Coding

3.5. Digital I/O

MF 624 contains one 8-bit digital input port and one 8-bit digital output port. Digital input port can be accessed directly by read from DIN register. Inputs are TTL compatible. Digital output port can be accessed by byte or word write to DOUT register. Outputs are TTL compatible. After power-on or hardware reset digital outputs are set to 0.

3.6. Quadrature Encoder Inputs

MF 624 contains four quadrature encoder inputs with single-ended or differential interface and index inputs. Inputs are differential TTL compatible with Schmitt triggers.

MF 624 can be used either with single-ended or differential encoder outputs. In case of single-ended encoder outputs use + signal inputs and leave - inputs disconnected. If differential encoder outputs are used connect both + and - inputs of MF 624 to encoder outputs. In both cases connect encoder signal ground to GND on X2 connector of MF 624.

Each IRC channel has one 32 bit data register IRC0 - IRC3. Control and status

registers IRCCTRL and IRCSTATUS are common for all IRC channels. Each IRC counter can be switched to bidirectional counter mode. In such case A is clock input and B controls direction (1 up, 0 down). In IRC and counter modes counter reset can be controlled by I input.

3.7. Timer/Counter

MF 624 contains 5 timers/counters with 50 MHz clock. The first four timers are accessible through external connector X2 while the fifth timer can generate system interrupt or trigger A/D conversion, or can be used as a clock source for other timers or for similar internal functions. TxIN pin on I/O connector can serve either as clock, gate or trigger input depending on configuration. Inputs and outputs are TTL compatible, Schmitt triggers are at all inputs to improve noise immunity.

Counters are implemented in programmable gate array chip offering wide range of operation modes allowing:

- up/down, binary counting
- internal or external clock and gate sources
- prescaling
- one shot/continuous outputs
- software/external triggering
- programmable gate and output polarities
- pulse counting
- frequency measurement
- pulse generation including PWM
- programmable clock source

4. I/O Signals

4.1. Output Connector Signal Description

The MF 624 multifunction I/O card is equipped with an on-board 37 pin D-type female connector X1 and with an aditional 37 pin D-type female connector X2 on cable extender. For pin assignment refer to Tables 24 and 25. TB 620 Terminal Board can be connected to both connectors.

AD0-AD7	Analog inputs
DA0-DA7	Analog outputs
DIN0-DIN7	TTL compatible digital inputs
DOUT0-DOUT7	TTL compatible digital outputs
IRC0-IRC3	Quadrature encoder A, B and Index inputs
T0IN-T3IN	Timer/counter gate and clock inputs
T0OUT-T3OUT	Timer/counter outputs
TRIG	A/D converter external trigger input
+12V	+12V power supply
-12V	-12V power supply
+5V	+5V power supply
AGND	Analog ground
GND	Digital ground

AD0	**1**	**20**	DA0
AD1	**2**	**21**	DA1
AD2	**3**	**22**	DA2
AD3	**4**	**23**	DA3
AD4	**5**	**24**	DA4
AD5	**6**	**25**	DA5
AD6	**7**	**26**	-12V
AD7	**8**	**27**	+12V
AGND	**9**	**28**	+5V
DA6	**10**	**29**	GND
DA7	**11**	**30**	DOUT0
DIN0	**12**	**31**	DOUT1
DIN1	**13**	**32**	DOUT2
DIN2	**14**	**33**	DOUT3
DIN3	**15**	**34**	DOUT4
DIN4	**16**	**35**	DOUT5
DIN5	**17**	**36**	DOUT6
DIN6	**18**	**37**	DOUT7
DIN7	**19**		

Table 24. X1 Connector Pin Assignement

IRC0A+	**1**	**20**	IRC3A+
IRC0A-	**2**	**21**	IRC3A-
IRC0B+	**3**	**22**	IRC3B+
IRC0B-	**4**	**23**	IRC3B-
IRC0I+	**5**	**24**	IRC3I+
IRC0I-	**6**	**25**	IRC3I-
IRC1A+	**7**	**26**	TRIG
IRC1A-	**8**	**27**	
IRC1B+	**9**	**28**	+5V
IRC1B-	**10**	**29**	GND
IRC1I+	**11**	**30**	T0IN
IRC1I-	**12**	**31**	T0OUT
IRC2A+	**13**	**32**	T1IN
IRC2A-	**14**	**33**	T1OUT
IRC2B+	**15**	**34**	T2IN
IRC2B-	**16**	**35**	T2OUT
IRC2I+	**17**	**36**	T3IN
IRC2I-	**18**	**37**	T3OUT
GND	**19**		

Table 25. X2 Connector Pin Assignement

Contact address:

HUMUSOFT s.r.o.
Pobřežní 20
186 00 Praha 8
Czech Republic
tel.: + 420 2 84011730
tel./fax: + 420 2 84011740
E-mail: info@humusoft.com
Homepage: http://www.humusoft.com