Time-to-Digit Converter Based on Radiation-Tolerant FPGA

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***Abstract*— Architecture of a time-to-digit converter (TDC) is presented. TDC is an electronic device which measures time of arrival of discrete electronic pulses, with respect to reference time base. Our work on TDC is motivated by its applications in field of long-range laser distance measurement and time synchronization. Unlike earlier time interpolation methods, we have chosen all-digital approach based on pulse propagation through tapped delay line. We do not expect it could outperform recent invention of time interpolation using narrow-band filter excitation [1], [2]. However, our approach relies on a standard digital circuitry only. With space applications in mind, we are implementing the TDC into a space qualified, radiation-tolerant field-programmable gate array (FPGA). On top of related works [4] and [5] on all-digital TDCs, delay line, we try to gather more complete information about the sampled pulse. It is done by sampling of whole bit vector, corresponding to all of the delay line taps. A calibration method based on random pulse source is discussed, including preliminary results. Impact of physical FPGA cell placement on resulting time measurement granularity is observed. Actually measured jitter distribution is compared to normal distribution function, giving an insight of absolute accuracy limit of our approach within the given FPGA platform.**

I. Introduction

General principle of time-to-digit conversion is as follows. Ticks of a high stable and low noise reference clock is counted by a digital counter. In this manner, time can be measured in chunks of reference clock period, which is, however, insufficient if precision higher than clock period is required. For this reason, time interpolation is employed while measuring times with resolution higher than clock period.

The digital approach employs tapped delay line on which the incoming pulse propagates. Each part of the line is sampled regularly by reference clock and the pulse position determines time elapsed since previous clock tick. The delay line can be either active or passive. Active line is formed by chain of active elements with defined delay such as buffers, latches, multiplexers, or gates [3].

The passive delay is formed purely by a ”slow” wire structure without any active element [5]. Thereby the jitter of delay elements is eliminated and only jitter of sampling elements remains. Less significant aging and temperature influence on TDC performance is expected, too. Moreover, each part of the delay line could have much lower delay (thus finer resolution) than any active component. The goal is to reach such a resolution that the limiting factor will be the jitter of the sampling elements. In order to obtain relevant data, it is necessary to ensure that the clock signal will propagate much faster than incoming pulse signal traveling through passive delay line to data inputs of sampling elements.

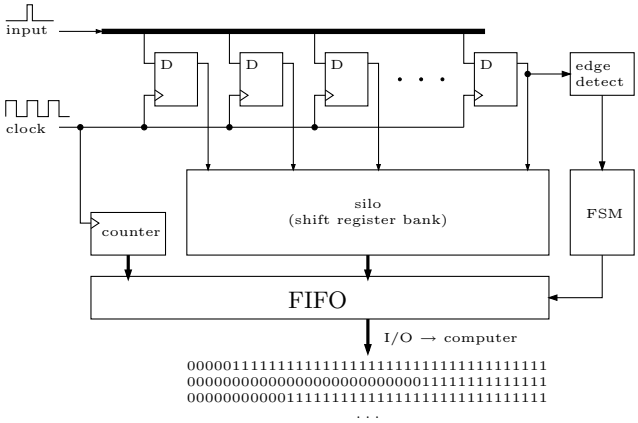

Fig. 1. TDC block diagram

II. Design

The TDC concept being presented (Fig. 1) employs passive delay line naturally offering the best possible line granularity thus theoretically the ultimate TDC resolution in a given FPGA technology. The pulse to be measured propagates from an input through the passive line which is connected to a number of D-type flip-flop inputs sampling (snapshotting) the line on clock edge. The position, spacing, and number of flip-flops are crucial aspects affecting the TDC precision and linearity. The outputs of the snapshotting flip-flops are connected to bank of parallel shift registers, called ”silo”. In other words, there is a cascade of flip-flops where bit information from a top level flip-flop (directly connected to the delay line) propagates through multiple levels of silos to the bottom flip-flops to be serialized into FIFO memory. Alternatively, the outputs of the snapshotting flip-flops are summed to get the total number of flip-flop ”ones” thus not preserving the whole bit vector. The advantages of the adopted principles are pure digital approach (standard FPGA/CMOS), scalability (the more flip-flops the better precision), implementation in a single principal component, and availability of radiation-tolerant FPGA for space applications.

978-1-4673-1923-2/12/$31.00 ©2012 IEEE

III. Calibration

A calibration is necessary in the case of TDC using passive delay line implemented within FPGA. Since there is little control over FPGA net routing, there is no prior knowledge of actual tap delays. The non-linearity issue may be overcome by employing a random pulse source as a base for stochastic calibration. It is beneficial compared to deterministic calibration since it provides in-situ (on-board) stability check and long-term recalibration (drift, aging). Provided the reference clock is accurate, a huge amount of pulses arriving at random times is able to provide sufficient data for calibration by histogram. The non-linearity compensation uncertainty after N_{RE} random events (negligible jitter assumed [1]) is defined as

$$\sigma_t = \frac{T_0}{2\sqrt{N_{RE}}} \tag{1}$$

where T_0 is the total delay of the line. The calibration by histogram is based on following assumptions: the frequency of reference clock is defined and stable, incoming pulses have known probability distribution in time, and the sample set of pulses is sufficiently large and representative. The most likely and simplest assumption is that pulse event time within one clock period follows uniform probability distribution ($t \sim \mathcal{U}(0, T_0)$), where T_0 is reference clock period and t is pulse arrival time modulo T_0.

After collecting huge amount of data, a histogram is created. Each pulse yields a bit vector of length M, corresponding to M taps of delay line. The sum of all bit vectors gives the histogram of M bins.

A. Random Pulse Sources

Simple and efficient realization of the random pulse source is made by using oscillator with large phase-noise ($t \sim \mathcal{U}(0, T_0)$), which is unrelated in frequency and not coupled by any means to the reference clock oscillator. The reference clock used was a crystal oscillator, while the random pulse source has been an RC astable generator formed around NE555 chip. The care was taken to isolate NE555 from the FPGA and crystal oscillator. Independent power supplies have been used. The configuration is depicted in Fig. 2.

Alternatively, a single photon avalanche diode (SPAD) may be adopted as a random pulse source. There are two modes of operation in case of SPADs. Either it generates uniformly distributed pulses ($t \sim \mathcal{U}(0, T_0)$) in non-gated mode, or the SPAD is coherently gated with clock exhibits exponential-like distribution having origin in background thermal or photoelectric events.

IV. Performance

There are two main uncertainty factors determining the TDC precision. The major factor is the maximum inter-tap delay, i.e. a delay line granularity. It may be reduced by increasing the number of line taps (N); thus, it decreases as $\frac{1}{N}$. The second perturbation phenomenon comes out from the flip-flop jitter including metastability. This factor is reduced as $\frac{1}{\sqrt{N}}$. Currently, our design is still limited by the inter-tap delay.

[1]The presence of jitter tends to smooth histogram by occurrences of "leap" bit vectors, such as ...00010111..., ...000100111... etc. which cause systematic error in histogram. Calibration jitter estimation and compensation methods are under development.

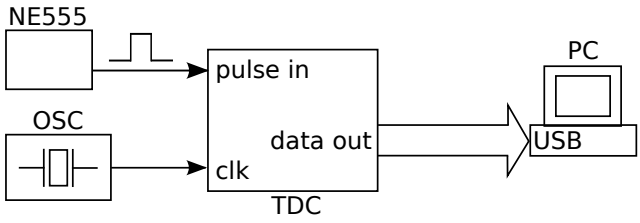

Fig. 2. TDC calibration setup

The worst-case deterministic error may be expressed as follows

$$\Delta t_{max} = \frac{1}{2} \max_k \Delta t_k, \tag{2}$$

where Δt_k is delay of k-th tap element. Root mean square (RMS) deterministic error is calculated under the assumption of uniformly distributed pulse epochs ($t \sim \mathcal{U}(0, T_0)$) as follows

$$\Delta t^2_{RMS} = \frac{1}{12 T_0} \sum_{k=1}^{N} \Delta t_k^3 \tag{3}$$

A. Topology (FPGA floor-plan) impact on inter-tap delay

The first delay line topology was formed as a horizontal straight line across the FPGA floor-plan. Besides it is constituted from relatively small number of flip-flops (320), it suffers from the fact that the tapped line crosses structural boundary of the FPGA floor-plan giving about an order of magnitude times higher propagation delay in the case of the boundary taps compare to the same net between an adjacent flip-flops. These non-uniform inter-tap delays result in the strong regions of non-linearity depicted in Fig. 3. The worst-case deterministic error of the 320-tap topology is $\Delta t_{max} = 87.6\,\text{ps}$ and $\Delta t_{RMS} = 24.8\,\text{ps}$.

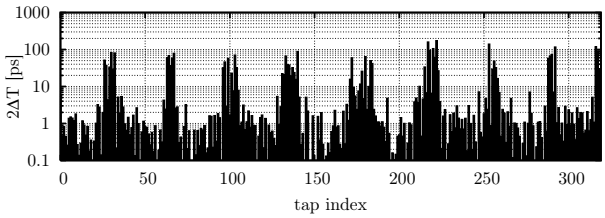

Fig. 3. TDC delay line topology consisting of 320 taps

Consequently, an optimized tapped delay line design was proposed where 2700 flip-flops are nearly equidistantly distributed around the FPGA floor-plan giving $\Delta t_{max} = 20.7\,\text{ps}$ and $\Delta t_{RMS} = 3.03\,\text{ps}$, respectively.

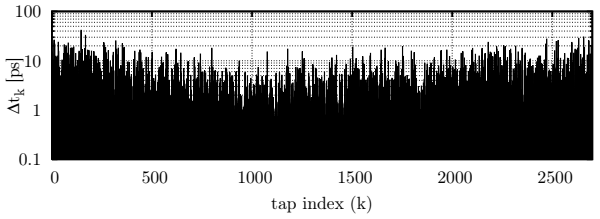

Fig. 4. TDC delay line topology consisting of 2700 taps

V. Results

There has been performed several experiments testing the performance of the device. Block diagram of configuration in which a delay generator has been employed is shown in Fig. 5.

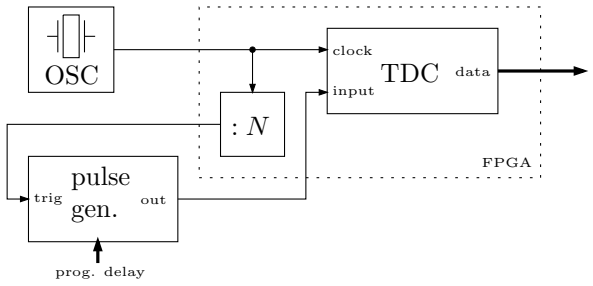

Fig. 5. Test measurement using delay generator

The delay generator was triggered by reference clock and produced several programmed delays with respect to the sampling clock; thus, arbitrary part of the TDC delay line could be verified. For each preset delay on pulse generator, a set of impulses was recorded and a histogram calculated. Each data set is plotted with respect to absolute time axis as bin numbers was already calibrated. Normalized cumulative histograms (NCH) for each data set are plotted in Fig. 6. Each NCH is an approximation of cumulative distribution function (CDF) of pulse arrival time, as measured by calibrated TDC.

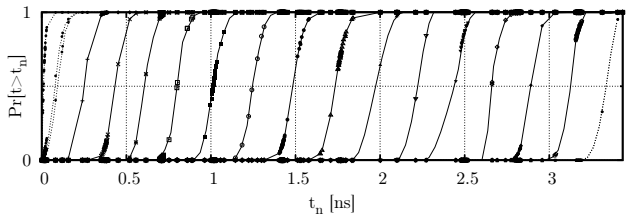

Fig. 6. Normalized cumulative histograms approaching pulse delay CDF

In ideal case of zero jitter, the CDFs would be straight vertical $0 \rightarrow 1$ steps residing at measured time delay. The S-shaped slope of measured CDFs is caused by jitter. The uneven spacing of "sampling points", i.e., histogram bins, is of no surprise, since it consists of peaks and valleys (Fig. 3). Mean observed time delay should lie in the center of CDF curve. Variation then corresponds to its slope. Due to sparsity of data points, we have assumed normal model of probability distribution and fitted each CDF with an error-function. After rejection of five data sets suffering from delay line boundary conditions, the agreement in fitted standard deviation σ among all NCH was better than 10%.

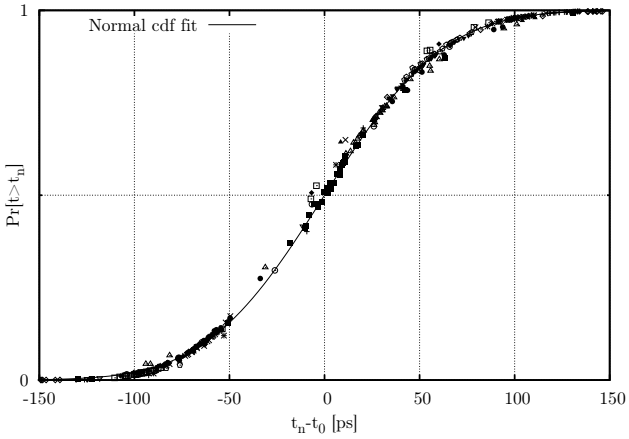

Fig. 7. CDF fit with measured data

Finally, the CDFs have been compared to the normal CDF model after subtraction of mean values, see Fig. 7 . Solid line represents true normal CDF with points of all NCHs superimposed. The overall agreement of fitted model and NHCs data points is 3 ps RMS. Standard deviation of the model is 49 ps RMS, which match the pulse generator specification being 50 ps.

Other experiment configurations has shown that the second largest jitter contributor (after pulse generator itself) is on-chip PLL. Additionally, jitter added by FPGA circuitry to a signal simply passing through the chip without any intended interaction was determined to be 2 ps RMS. Considering this facts, another configuration, omitting both main jitter contributors, was employed during tests.

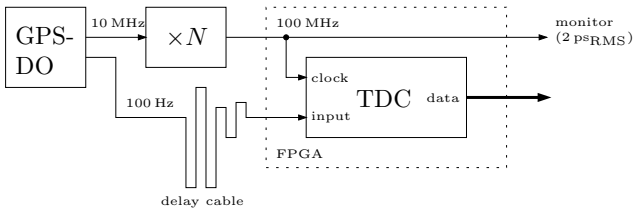

Fig. 8. Test measurement using delay cable and signal distributor

The block diagram in Fig. 8 shows experiment setup where delay generator is substituted by a delay cable. Moreover, a 100 MHz signal directly from coherent multiplier serves as system clock thus the on-chip PLL was not utilized. The 10 MHz signal from GPS Disciplined Oscillator (TM-4) was divided by a signal distributor giving 100 Hz pulses synchronous with system/sampling clock. Employing delay cables with various lengths, various points of the delay line could be checked. Measured histogram of such a point can be seen in Fig. 9 which shows that the jitter in design without on-chip

PLL has been significantly reduced. Random jitter measured at one point of tapped line was $\sigma_j = 4.93\,\mathrm{ps}$, evaluated by standard RMS formula and line calibration method described above.

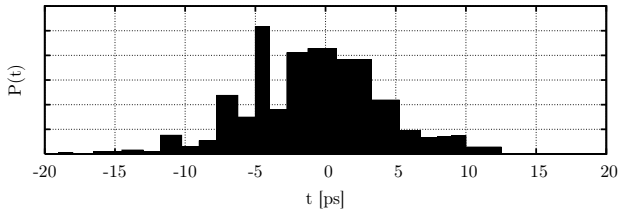

Fig. 9. Histogram data from a single point

VI. Conclusion

We have implemented several designs of TDC in single A3PE1500 FPGA by Actel/MicroSemi company, which has its radiation tolerant equivalent. The experiments show that the jitter of the TDC elements obeys normal distribution quite accurately (3 ps). The latest design exhibits worst-case deterministic error $\Delta t_{max} = 20.7\,\mathrm{ps}$, RMS deterministic $\Delta t_{RMS} = 3.03\,\mathrm{ps}$, and measured random jitter $\sigma_j = 4.93\,\mathrm{ps}$. The intended future experiments will focus on measuring the temperature and long term stability. The efforts in theoretical part will be concentrated mainly on evaluating impact of flip-flop metastability and also jitter self-estimation from whole bit vector data to improve histogram calibration.

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