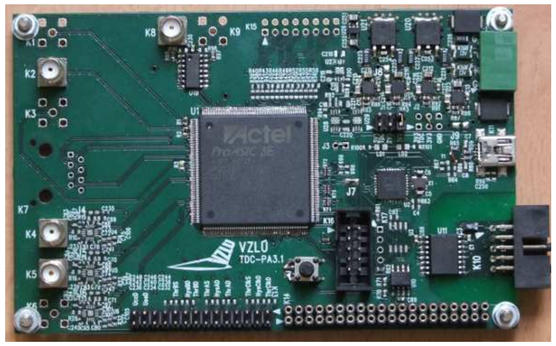
# Programmable Delay Controller Allowing Frequency Synthesis and Arbitrary Binary Waveform Generation

Marek Peca, Michael Vacek, Vojtěch Michálek
peca@serenum.cz
Výzkumný a zkušební letecký ústav, a.s., Beranových 130, Praha – Letňany, Czech Republic
České vysoké učení technické v Praze, Břehová 7, 115 19, Praha 1, Czech Republic

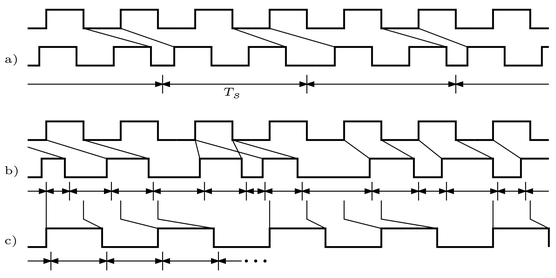
## Introduction

- Design of a programmable delay controller (PDC) within an aerospace-compatible, FLASH-based FPGA
- PDC for low-jitter arbitrary frequency generation
- Versatile PDC block capable of generating arbitrary binary waveform constrained only by minimum achievable edge-to-edge switching time
- Applications:
  - Frequency synthesis (DDS/PLL alternative)
  - Micro-phase stepper
  - Various modulators; all within purely digital circuit (FPGA, custom CMOS)



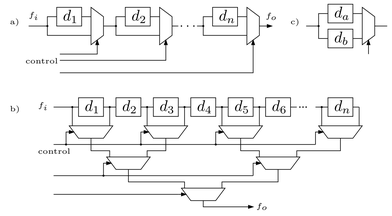

## Motivation

- Current PDC designs [1], [2], [3], [4], [5], [6] operate at $T_s \gg T_o$ (sampling period $T_s$ , time interval between the consecutive edges of output signal $T_o$)
- Our approach: seamless PDC operation at $T_s \to T_o$
  - Generation of arbitrary binary waveform constrained only by $T_o \geq T_s$,
  - Generation of arbitrary frequency, constrained by $f \leq \frac{1}{2 \cdot T_s}$,
  - Under proper treatment, no edge will be created by the switching elements themselves; therefore, the overall jitter will be composed solely of the jitter of input signal and propagation jitter of the delay elements.




## Delay line design

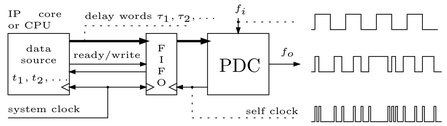
- Digital-based PDC consisted of fixed-length delay elements (transmission lines, gates) composed into signal path by electronic switches (multiplexers):
  - Linear
  - Tree-like
  - Differential delay ($d_a - d_b$) - very fine ($\sim$ ps) delay implementations



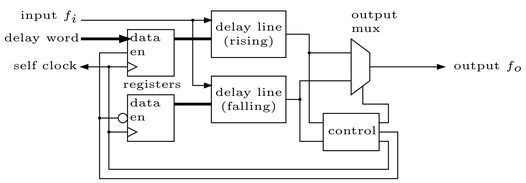

- $n$ delay cells providing fine granularity over all $2^n$ (element delays follow $\log_2$ distribution, $d_{k+1} = d_k/2$)
- Performance analysis - 13 bit cascaded structure (45 cells in total including multiplexers)
- Frequency synthesis scenario - 6 bit tree-like structure (idle delay mitigation)
- Implemented using SDF back-annotated files $\Leftarrow$ delay models of FPGA macros not available in open format

## Control logic design

- PDC operation in a self-clocked mode featuring standard asynchronous FIFO giving desired edge instants

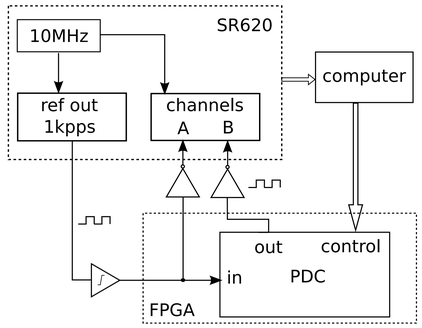


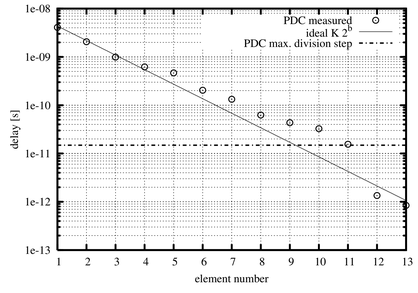

- Two identical delay lines (rising and falling edge propagation) avoiding glitches occurring during control input reconfiguration
- Asynchronous state machine generating non-uniform clock derived from delayed edges
- Unwanted (idle) delay between delay line reconfiguration instant and settling of output signal:
  - Linear structure $\sim \sum_{k=2}^{n} d_k$
  - Tree-like $\sim \log_2 T/h \cdot d_{multiplexer}$




## Resolution and jitter

- Time difference of reference signal split and connected to SR620 [7] (via PDC and directly via FPGA)
- 54 hours experiment duration, pseudo-random delay words intermixed with zero delay settings
- Total line delay $T = 8.72\,\text{ns}$, maximum step size between adjacent delay words $\Delta\tau_{max} = 14.9\,ps$

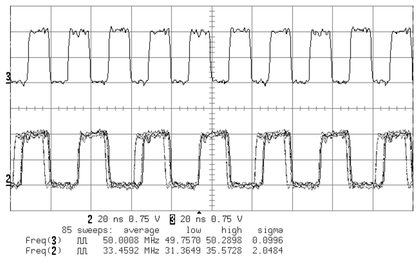



- Reference signal jitter $\sigma_{ref} = 1ps$ measured using NPET [8]
- Reference signal led via FPGA not passing PDC jitter $\sigma_{FPGA} = 2.9ps$
- Maximum and minimum propagation jitter $\sigma_{max} = 5ps$ and $\sigma_{min} = 4ps$ (all PDC delay elements on and off, respectively)

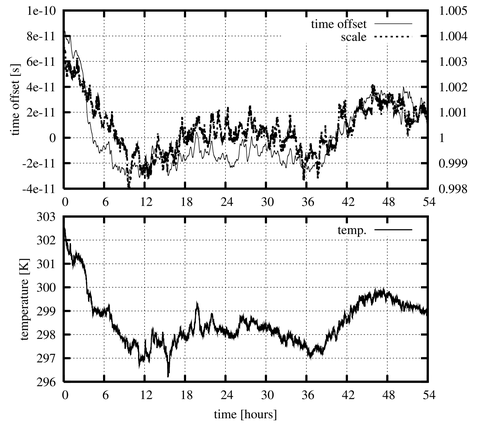
## Frequency synthesis

- Control logic concept-proof by performing the generation of $f_o = (2/3)f_i$ frequency ($f_o = 33.\bar{3}\,\text{MHz}$, $f_i = 50\,\text{MHz}$)




## Temperature drift

- Offset drift $23\,\text{ps}\,\text{K}^{-1}$ and scale drift $8.4 \times 10^{-4}\,\text{K}^{-1}$ yielding $30\,\text{ps}\,\text{K}^{-1}$ (linear approximation) in the worst case




## Conclusion

- Performance of 13 element PDC comparable to recent works [2] as well as to dedicated ECL circuits [4]
- Resolution improvement possible by adding more delay elements
- Temperature compensation possible by measurement of reference delay line element, e. g. using ring oscillator, or Time-to-Digital Converter [9].
- Significantly better performance achievable by ASIC implementation

## References

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