FPGA Based Testing of Hybrid Real-time Systems

Jan Krákora and Zdeněk Hanzálek

{krakorj,hanzalek}@fel.cvut.cz

Czech Technical University in Prague,

FEE, Department of Control Engineering

Karlovo náměstí 13, Prague 2, 121 35,

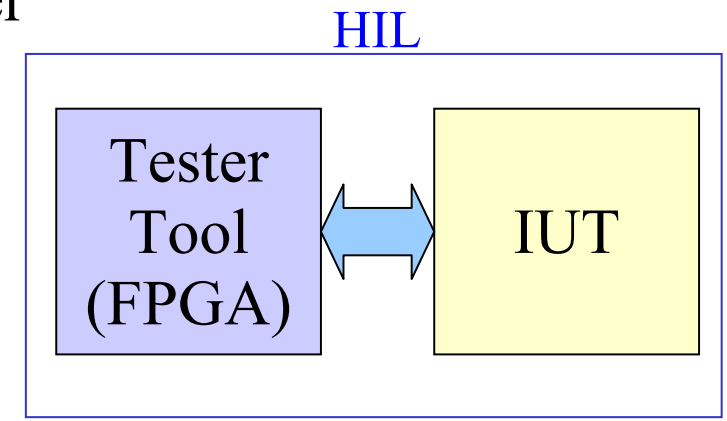
Czech Republic

Outline

- Introduction
- Motivation
- Tester tool structure
- Implementation
  - Continuous system
  - Discrete event system
- Case study
- Conclusion

Introduction

- Hardware-In-the-Loop (HIL)
  - Implementation Under Test (IUT)
    - technology process controller
    - automotive ECU, etc.
  - **Tester tool**
    - System model
    - Tester – case generator
    - Interfaces (verification I/O, HW I/O etc.)



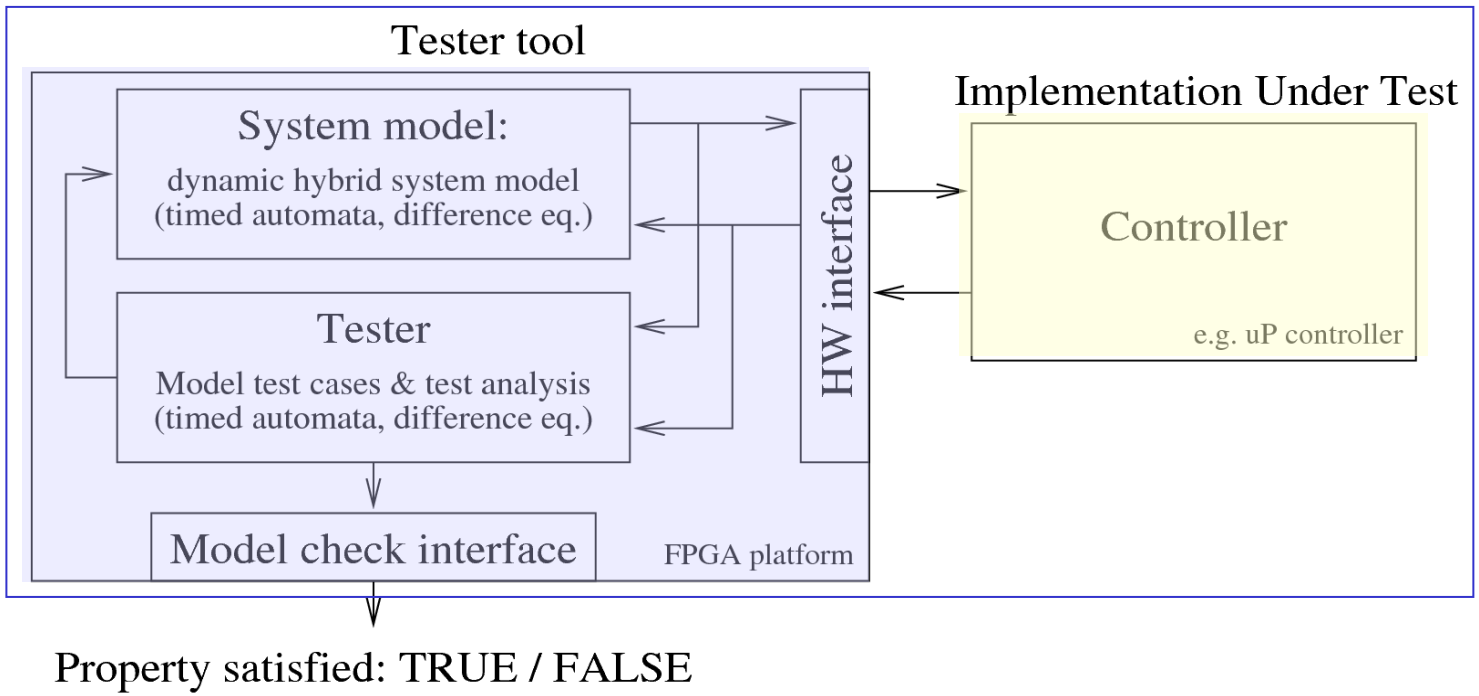
Motivation

- **New design methodology of TT**
  - **continuous** system (difference equation)
  - **discrete event** system (**timed automata**)
    - simple design
    - **verification using temporal logic**
    - **model checking**
      - logical, timed properties, deadlock free detection etc.
  - **FPGA** platform **use**
    - **speed** performance, **extensibility**, **time accuracy**
    - not influenced by upper layers (e.g. OS services)

Tester tool structure

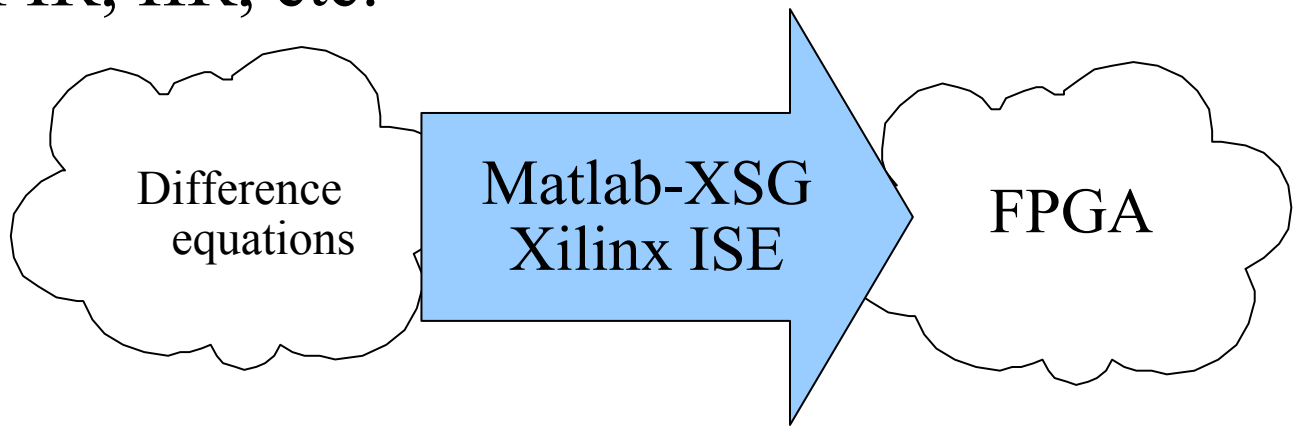
- System model
  - system specification
- Tester
  - Case generator
  - Analyzer
- HW interface
  - e.g. PWM, IRC
- MC interface

HIL



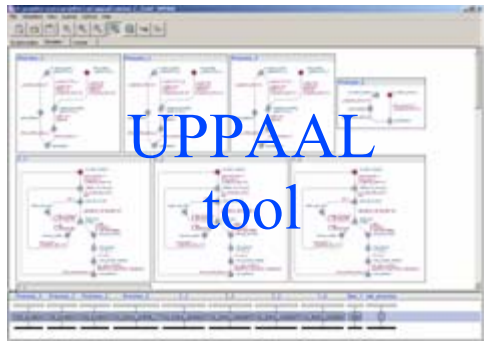
Continuous system implementation

- Discrete-time system
  - Difference equation
    - filter design and signal processing [Lutovac00]
- equation implementation => FPGA
  - FIR, IIR, etc.

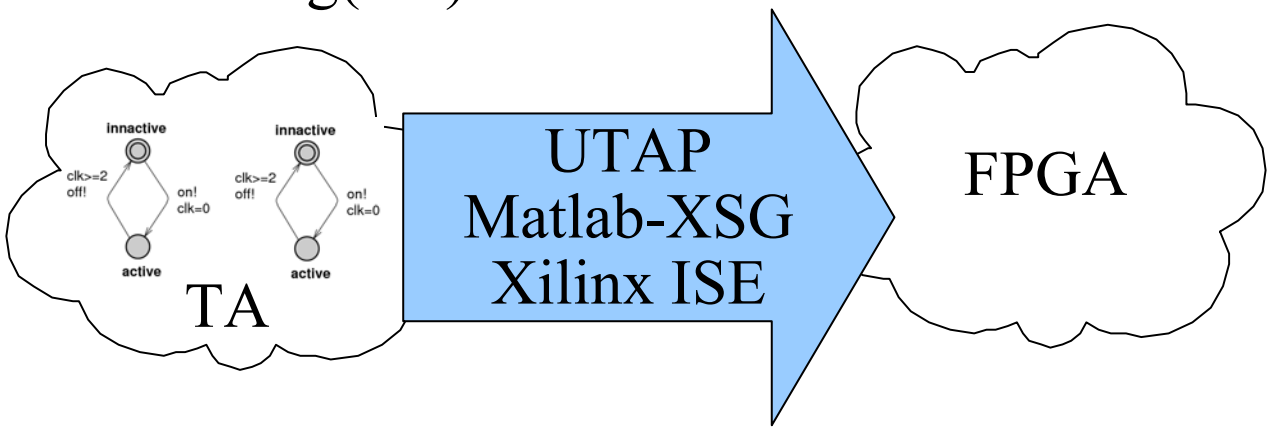


Discrete event system implementation

- Timed automata [Alur 94]
  - UPPAAL tool [Uppaal 02]
  - Verification using CTL

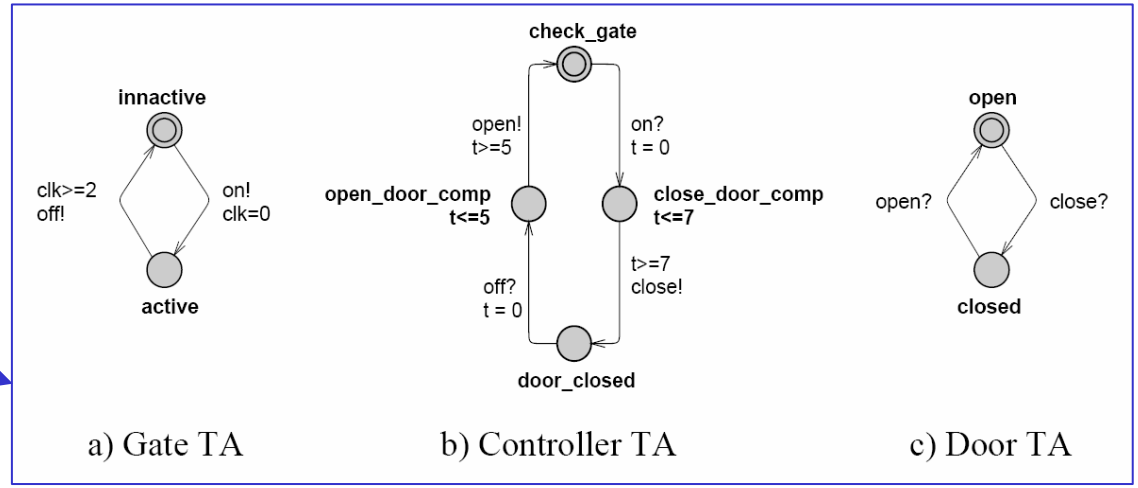


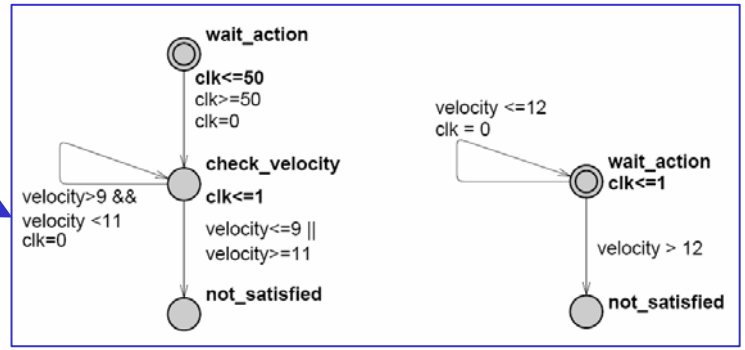
- Implementation TA => FPGA [Tripakis 05]
  - TA => Prog(TA)



Discrete event system implementation

- Why timed automata?
  - Discrete event system behavior description
  - Designing of observers for a tester
  - TA verification

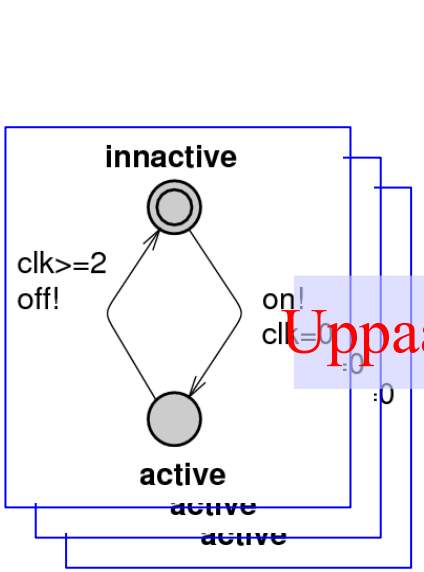




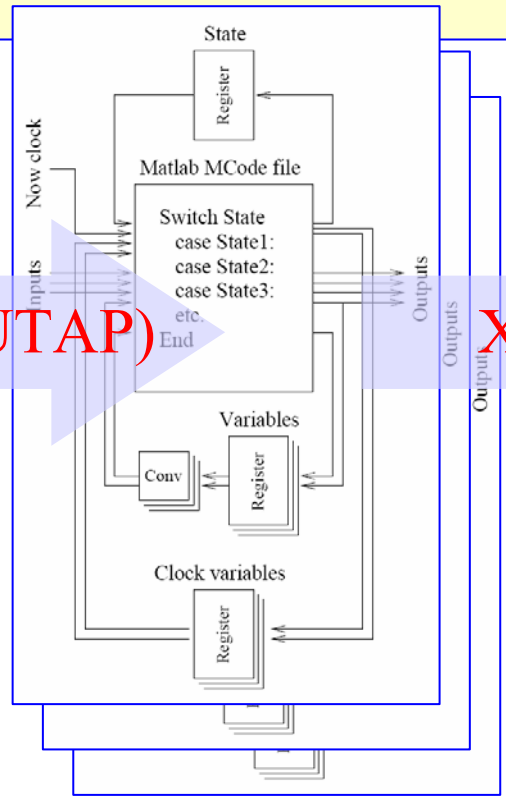
Discrete event system implementation

UPPAAL

Matlab/Simulink, Xilinx System generator



Uppaal2m (C++, UTAP)



Xilinx ISE

Case study – servo-system

- **Servo**-system
  - **without friction** to the shaft
  - **with friction**

$$G(z) = \frac{2.652z + 0.3143}{z^2 - 0.9202z + 0.0001003}$$

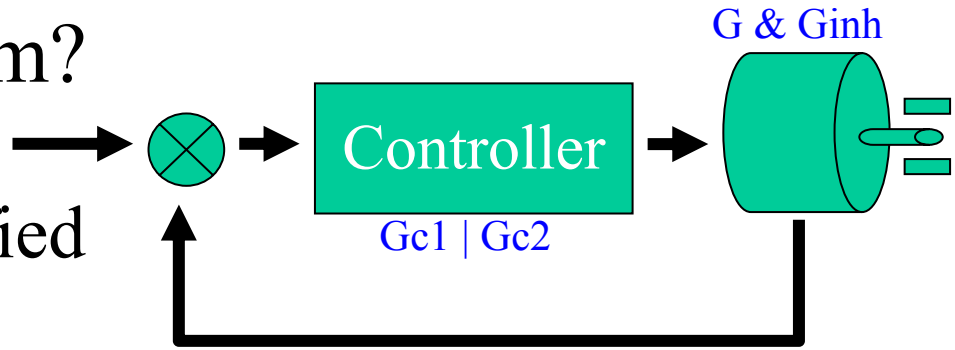
$$G_{inh}(z) = \frac{2.559z + 0.2924}{z^2 - 0.8483z + 9.249 * 10^{-5}}$$

- **Two controllers** to be tested

$$G_{C1}(z) = \frac{0.3136}{z + 0.5151}$$

$$G_{C2}(z) = \frac{0.3377z - 0.3056}{z - 1}$$

- Are given controllers able to control such system?
  - Test cases
  - Properties to be verified



Case study – servo-system

- Test cases
  - *[0; 20)* msec – motor with no friction
  - [20; inf) msec – motor with a friction

- Controller properties to be verified

  Property 1:

  The motor **angular velocity in interval (9,11)** Rads-1 **within 5 msec**

  For test case 1 only

  Property 2:

  The motor **angular velocity in interval (9,11)** Rads-1 **within 5 msec**

  For test case 2 only

  Property 3:

  The motor **angular velocity does not exceed 12 Rads-1**

  For test case 1 and 2 as well

Case study – servo-system

- Tester tool structure

Motor behavior

Continuous system

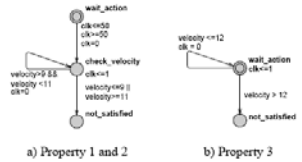
$$G(z) = \frac{2.652z + 0.3143}{z^2 - 0.9202z + 0.0001003}$$

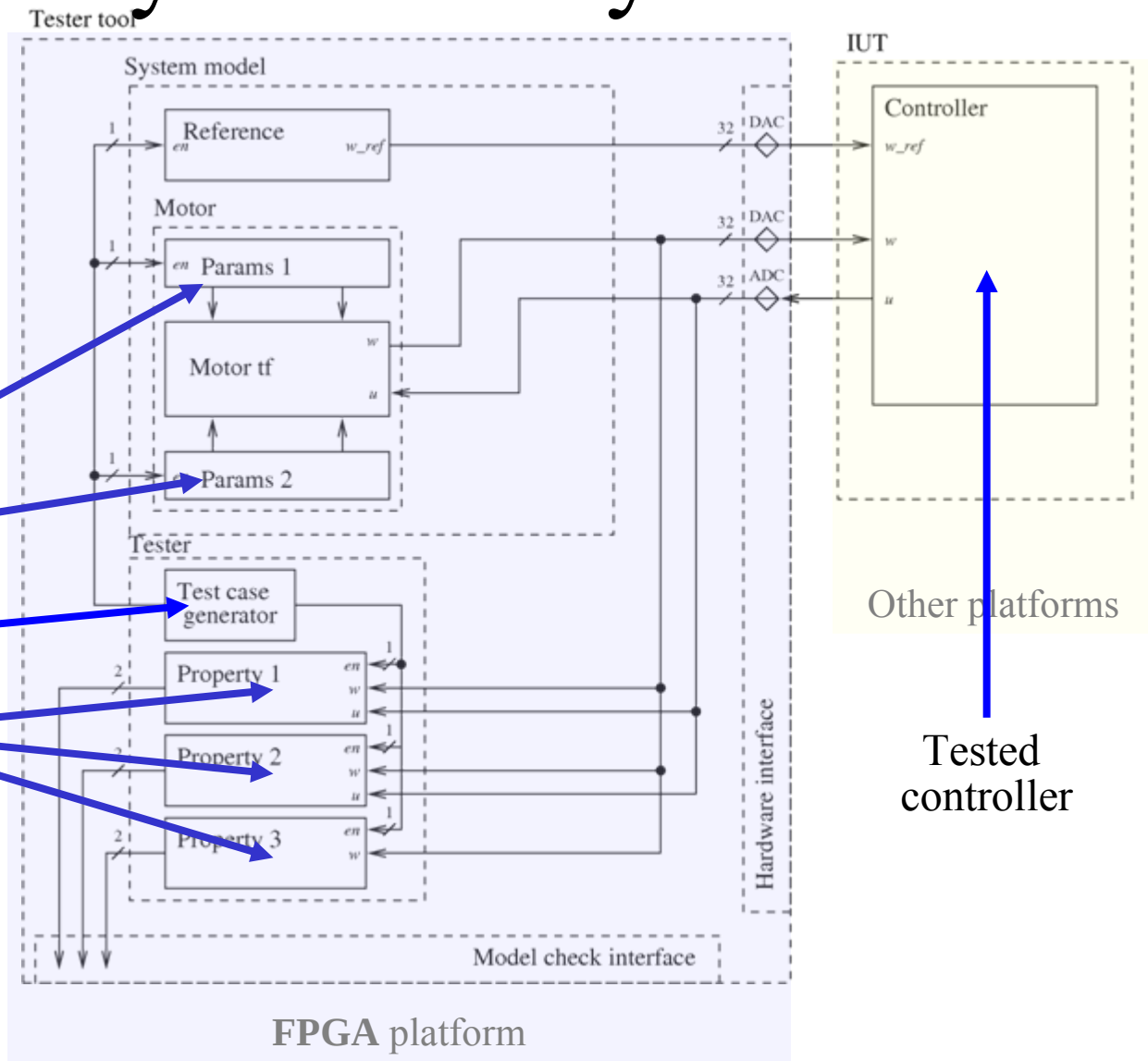
$$G_{inh}(z) = \frac{2.559z + 0.2924}{z^2 - 0.8483z + 9.249 * 10^{-5}}$$

Test case

Properties to be verified

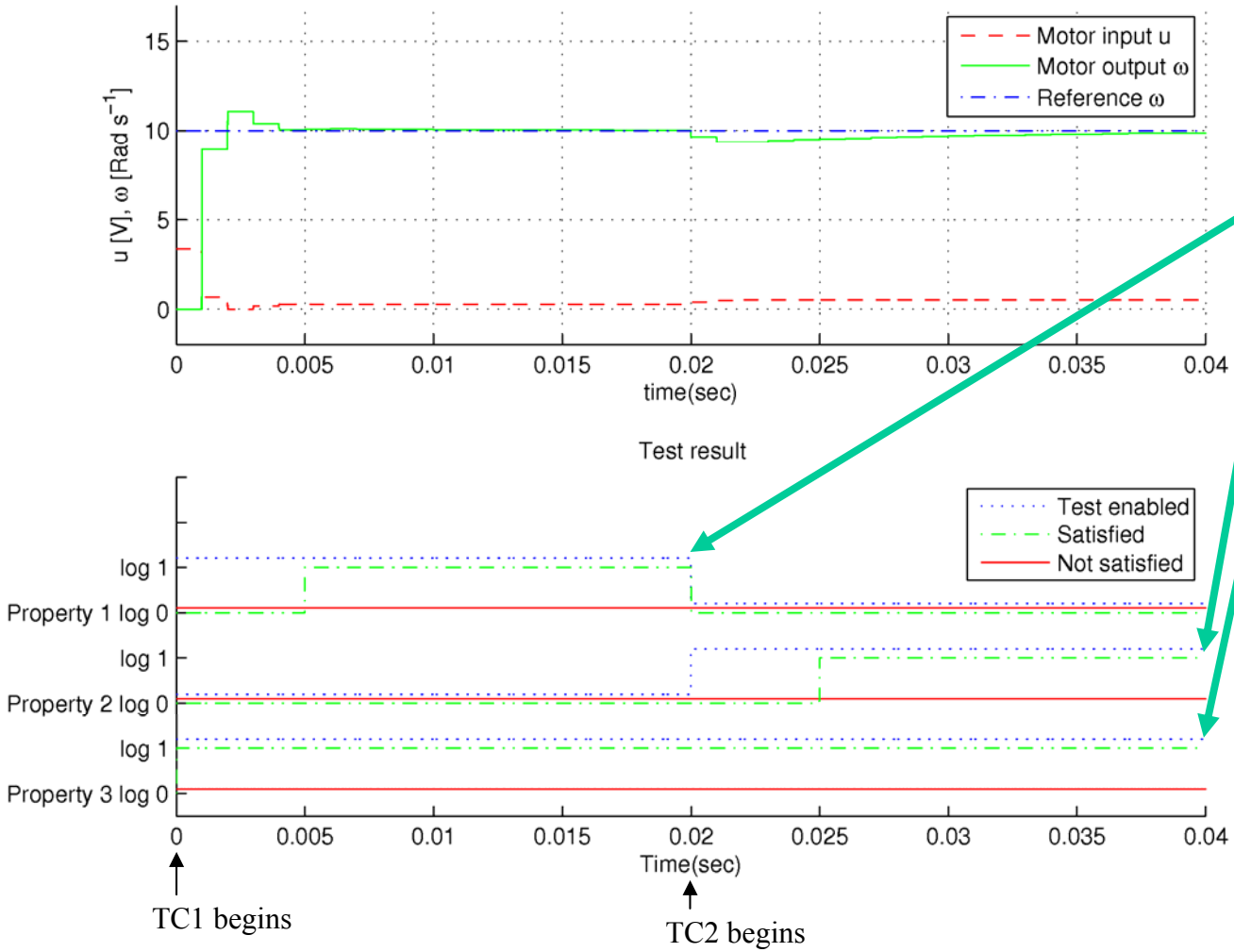
Discrete event system





Case study – servo-system

Controller 1 test results

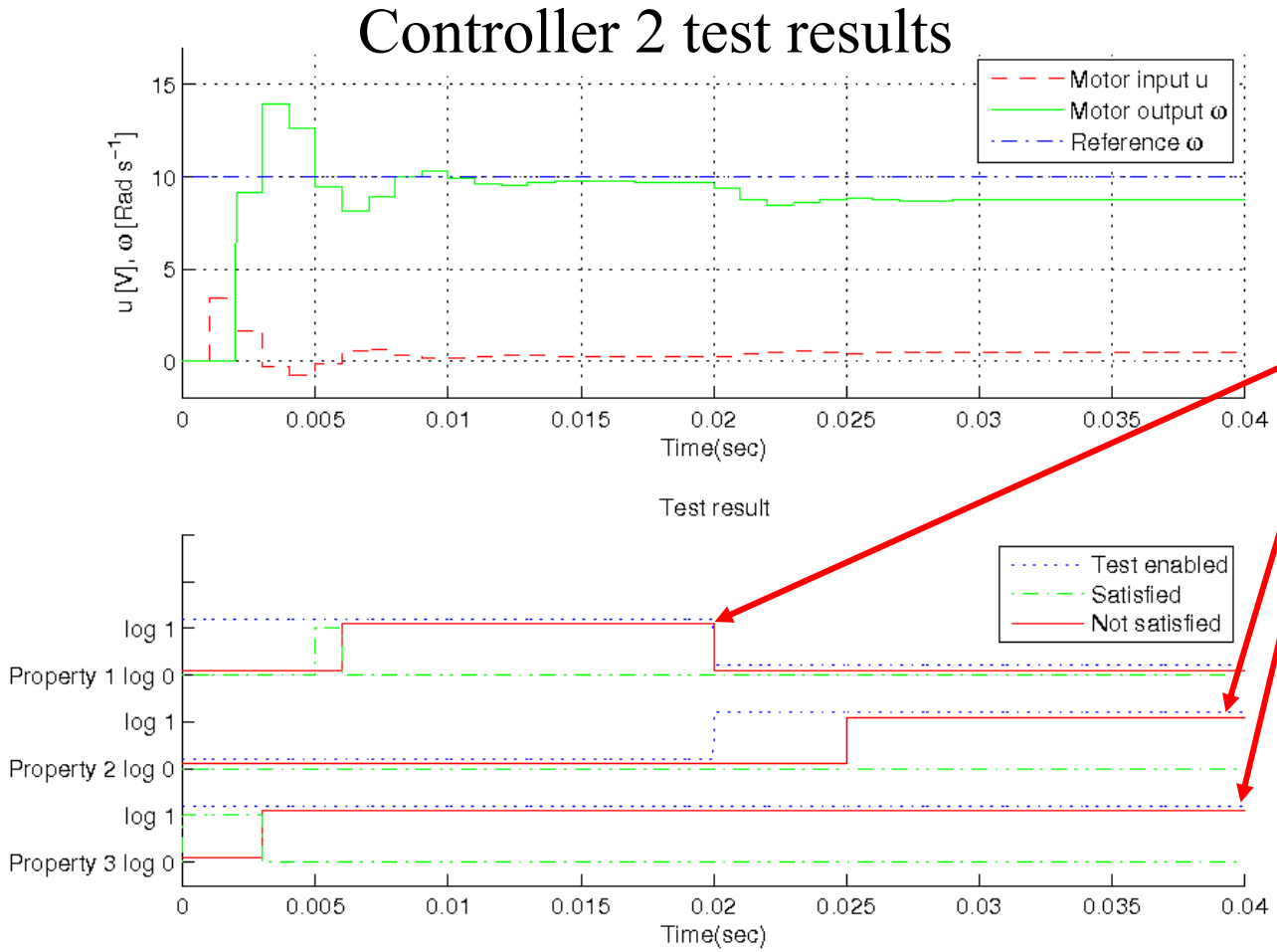


Property 1 - Satisfied

Property 2 - Satisfied

Property 3 - Satisfied

Case study – servo-system



Property 1 – Not satisfied

Property 2 – Not satisfied

Property 3 – Not satisfied

Conclusion & Further work

- Conclusion
  - **New design methodology of TT** into FPGA
    - High sampling period (nsec), Low jitter, Scalability, High degree of parallelism
  - **DES** based on **timed automata**
  - Testing framework speed performance
    - 100nsec (in compare to OS based testers)
- Further work
  - **Hardware interface improvement**
    - DAC/ADC, PWM, IRC etc.
  - Dynamic **reconfiguration of FPGA**
    - on-line generation of test cases
    - automation of testing process
  - Transformation tool improvement

Thank you for your attention

Jan Krákora and Zdeněk Hanzálek

{krakorj,hanzalek}@fel.cvut.cz

Czech Technical University in Prague,

Faculty of Electrical Engineering,

Department of Control Engineering

Karlovo náměstí 13, Prague 2, 121 35,

Czech Republic