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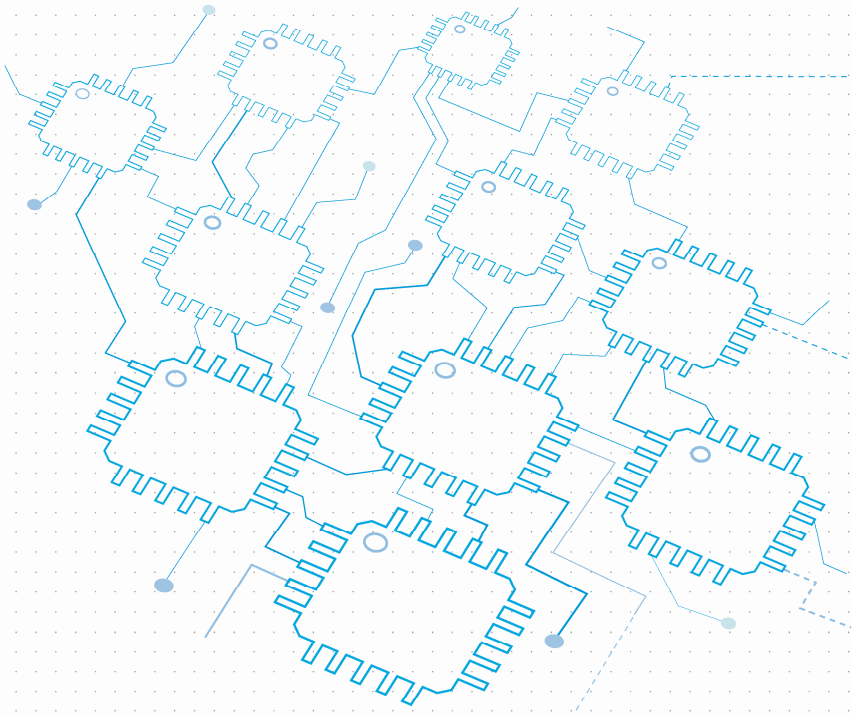
Institute of Information Theory and Automation



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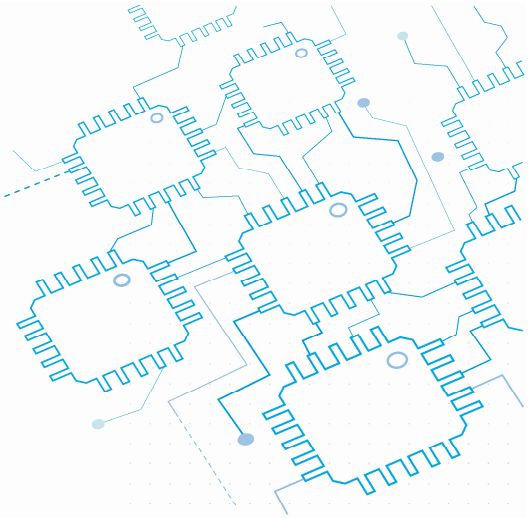
Partial Dynamic Reconfiguration in Xilinx FPGA Circuits

Lukáš Kohout

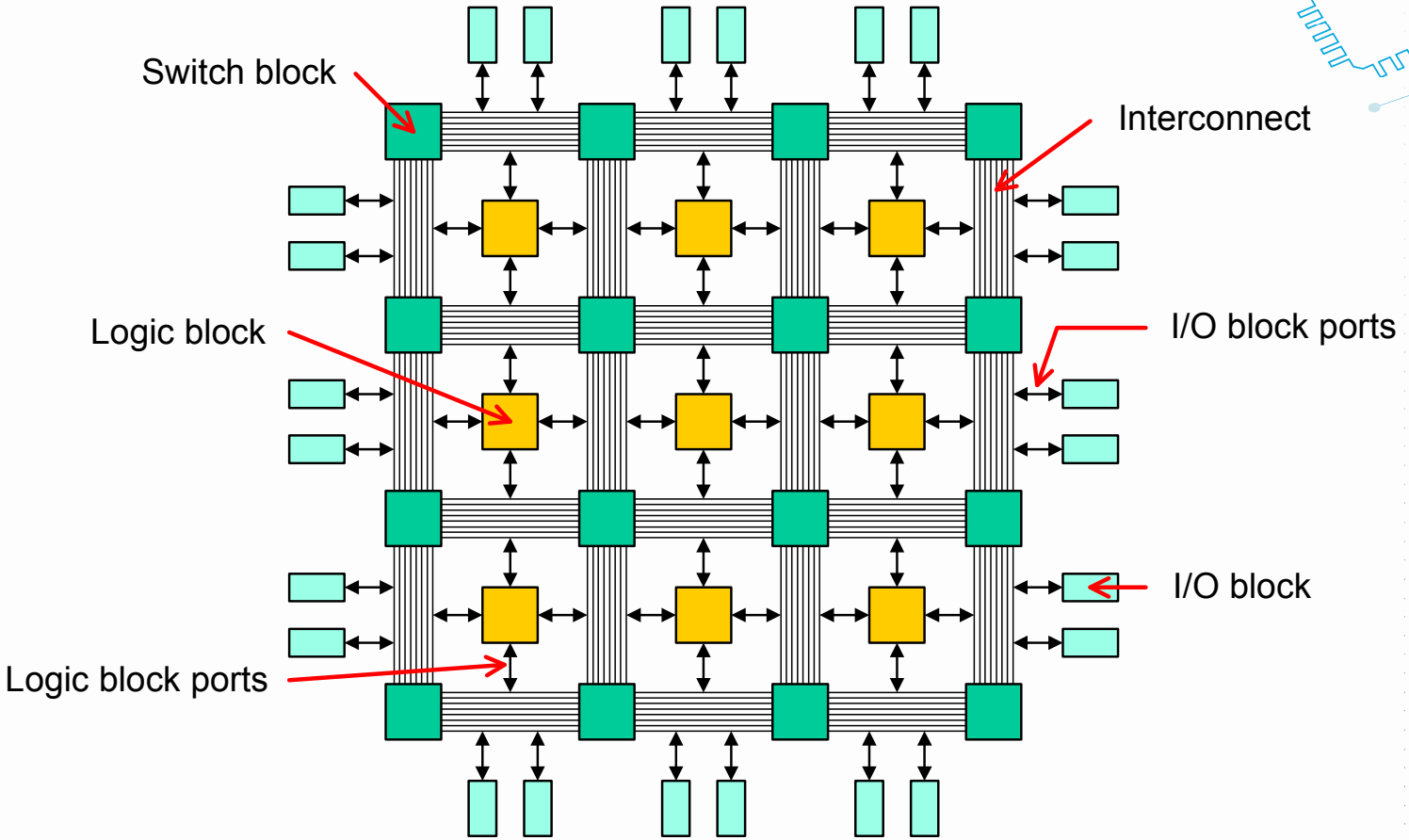
CAK Embedded Systems Colloquium 1.2.2007

Outline

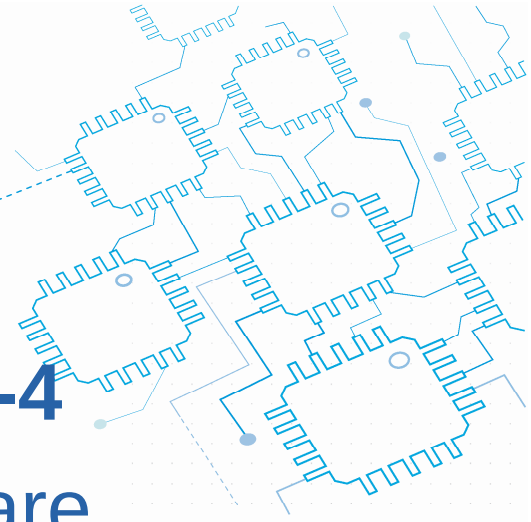


- FPGA architecture
  - logic blocks, interconnect resources
- Partial dynamic reconfiguration
  - Static and dynamic part, bus macros
  - Constraints
- Demonstrator
  - Reconfigurable FIR filter
  - MicroBlaze, System ACE, DDR, ICAP
  - Implementation - Xilinx ML402 platform

FPGA architecture



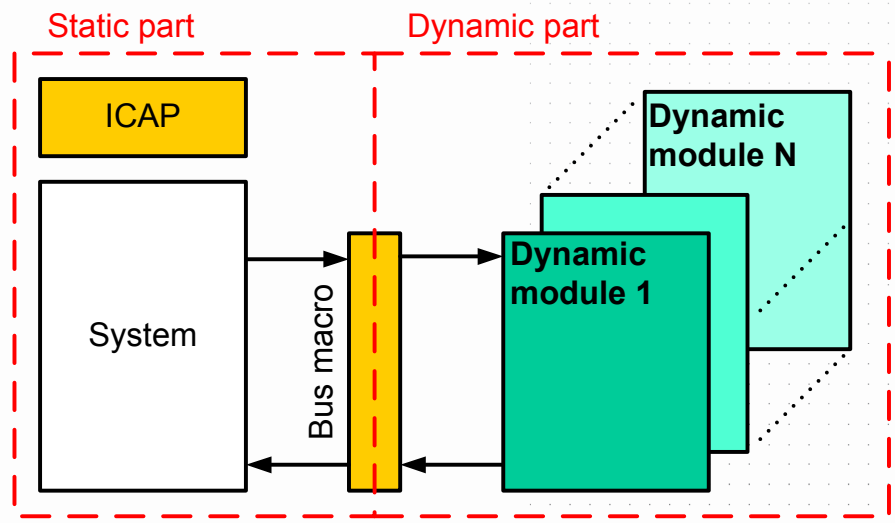
Partial Dynamic Reconfiguration



- Virtex™-II, Virtex-II Pro, and **Virtex-4**
- Multiple design modules to time-share physical resources
- Dynamic modules can be swapped on the fly
- Modular design required
- Dynamic modules with identical interface

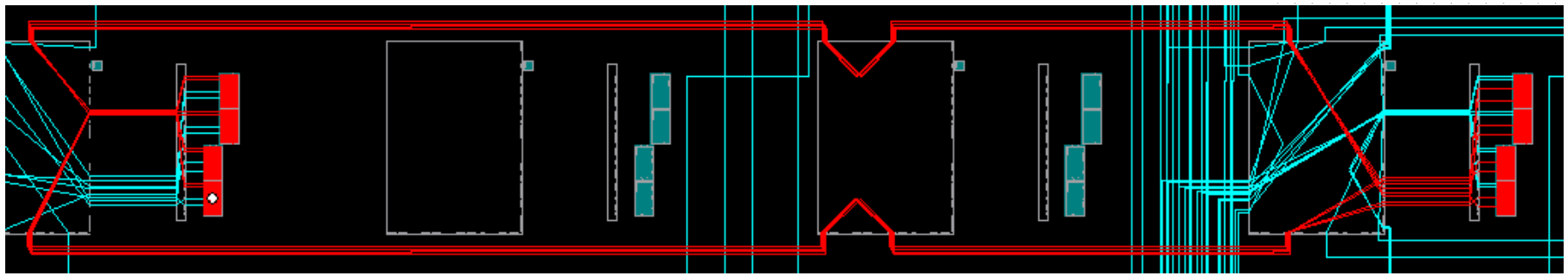
Static and Dynamic Part

- The static part is running all the time.
- The dynamic part is reconfigured on the fly.
- The interface between the static and dynamic part is formed by a bus macro.



Bus Macro

- Means of locking the routing between the dynamic and the static part
- All connections between the dynamic and static part must pass through a bus macro
- The clock signal is an exception



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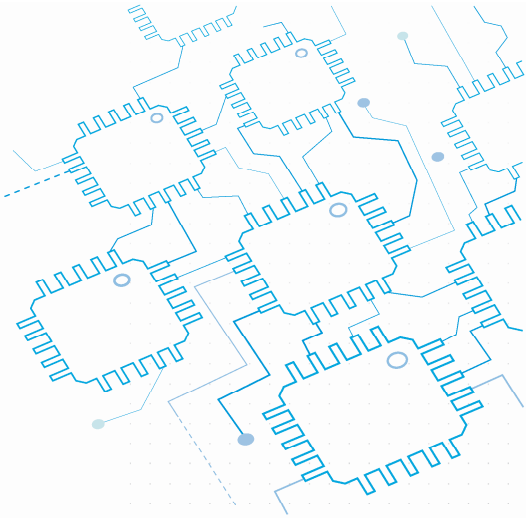
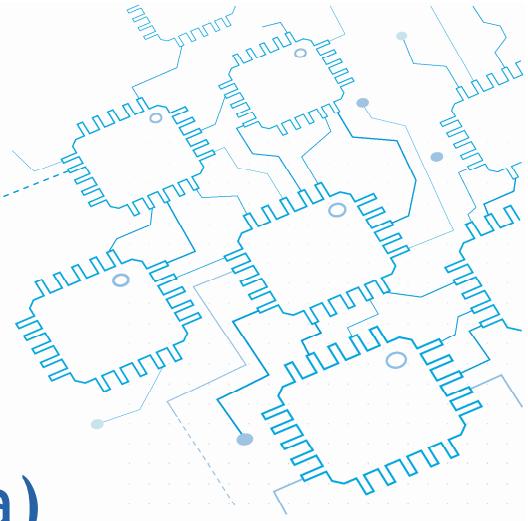
Constraints



- Knowledge of the placement
  - Static part
  - Dynamic part – can include more independent reconfigurable areas
  - Bus macros
- Specified in the *.ucf file

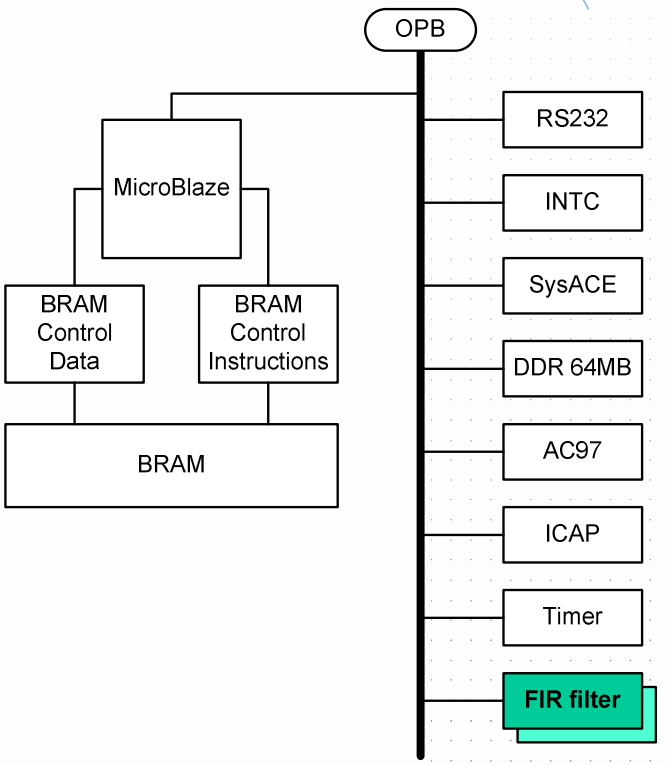
Demonstrator



- FIR filter
  - 16 bit sample/response (audio data)
  - 15 weights
  - Low pass filter (f_c = 4 kHz)
  - High pass filter (f_c = 4 kHz)
  - Sample rate = 44.1 kHz
- Xilinx ML402 evaluation platform
- MicroBlaze

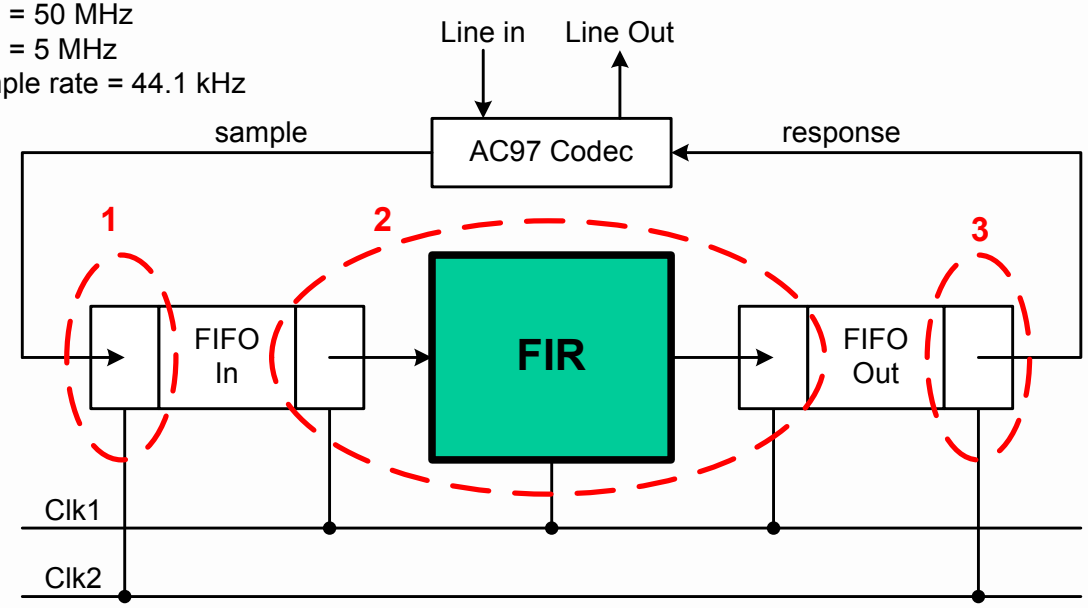
Demonstrator Description

- Static part
  - MicroBlaze
  - System ACE
  - DDR 64 MB
  - AC97 codec
  - ICAP - Internal Configuration Access Port
- Dynamic part
  - FIR filter



Data Flow

Clk1 = 50 MHz
Clk2 = 5 MHz
Sample rate = 44.1 kHz



1

```
if (new_sample)
 FIFO_In.write(sample)
```

2

```
if (FIFO_In.70_%_FULL)
  while(!FIFO_In.empty)
  {
    FIFO_In.read(sample)
    FIR.compute
    FIFO_Out.write(response)
  }
```

3

```
if (new_sample)
  FIFO_Out.read(response)
```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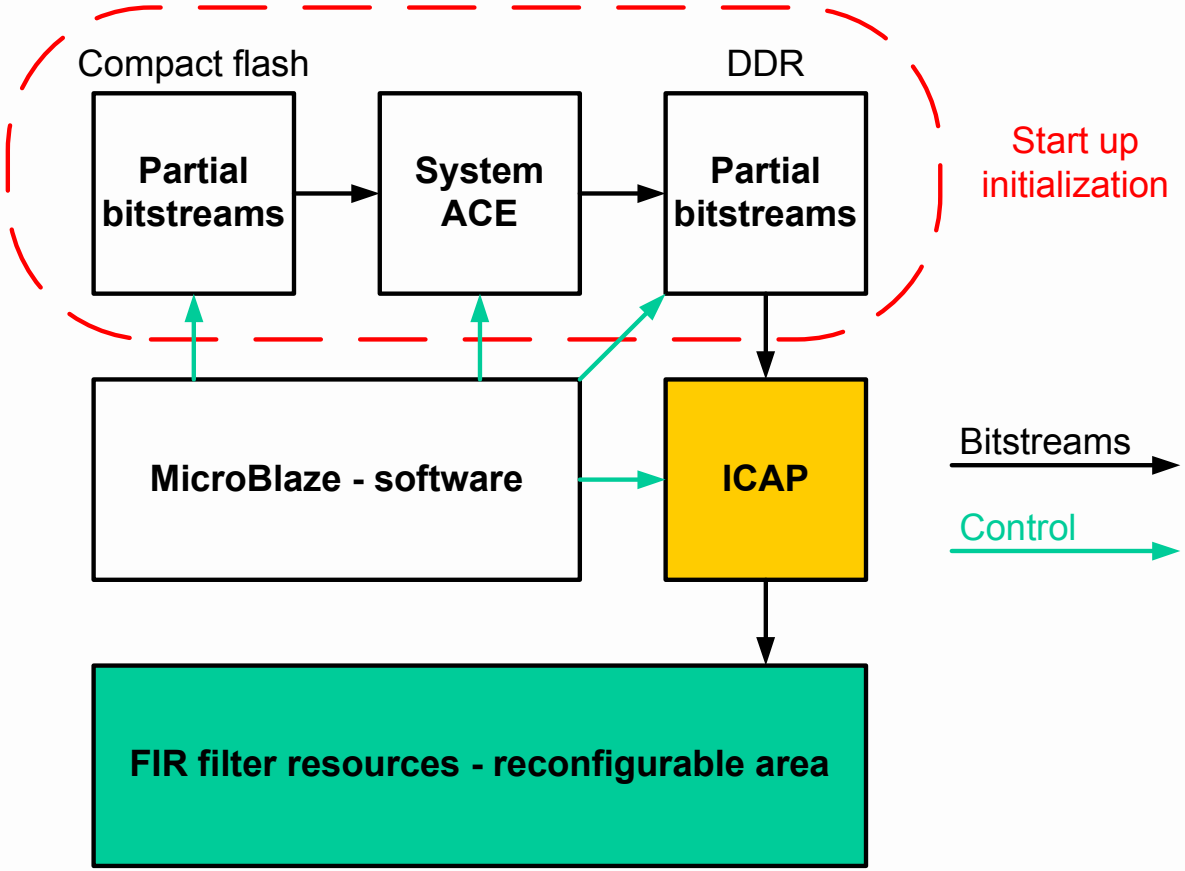
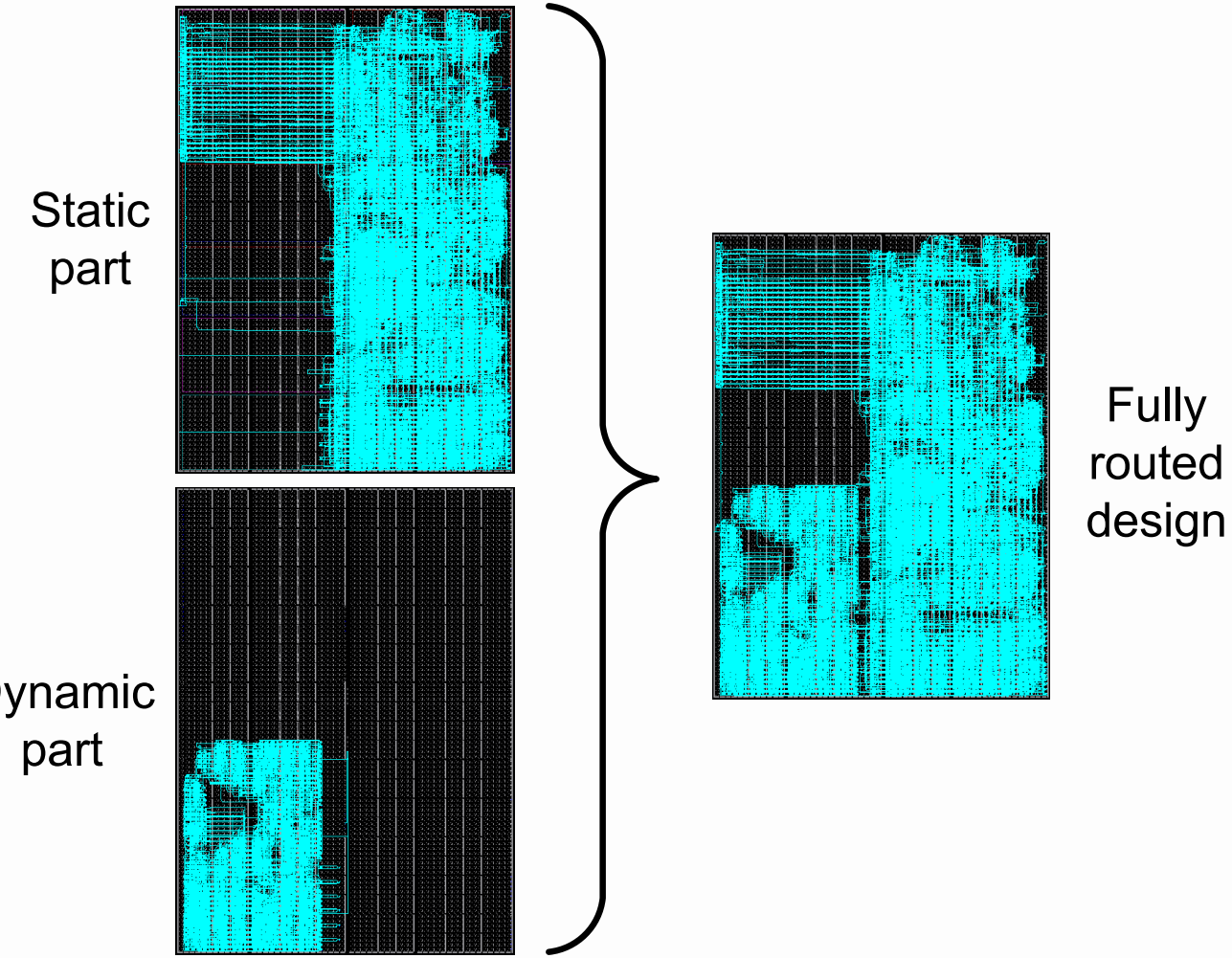
Reconfiguration Flow



Implementation

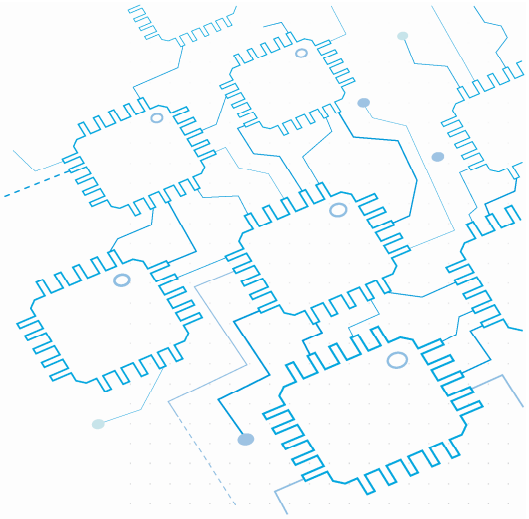


Implementation (2)

Used resources in Virtex-4 SX35

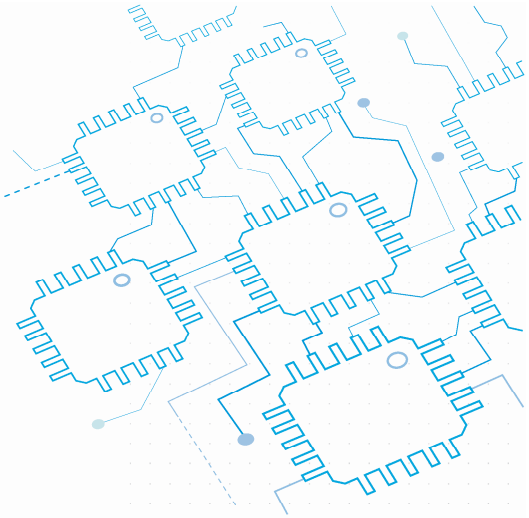
	Static	FIR HP	FIR LP	Total (fully static)	Total PR impl.	PR impl. vs. fully static
Number of Slice Flip Flops	4719	549	608	5876	5327	**9 %**
Number of 4 input LUTs	4359	3651	3480	11490	8010	**30 %**
Number of occupied Slices	4513	2318	2270	9149	6831	**25 %**
Total Number 4 input LUTs	5121	3831	3702	12654	8952	**29 %**
Number used as logic	4359	3651	3480	11490	8010	**30 %**
Number used as a route-thru	23	181	222	426	245	**42 %**
Number used for Dual Port RAMs	568	0	0	568	568	**0 %**
Number used as Shift registers	171	0	0	171	171	**0 %**
Number used as FIFO16s	0	0	0	0	0	**0 %**
Number used as RAMB16s	33	0	0	33	33	**0 %**
Number of DSP48s	3	0	0	3	3	**0 %**
Number of hard macros	6	0	0	0	6	**-100 %**
Number of ICAP_VIRTEX4s	1	0	0	0	1	**-100 %**
Total equivalent gate count for design	119334	47024	43840	210198	166358	**20 %**

Implementation (3)



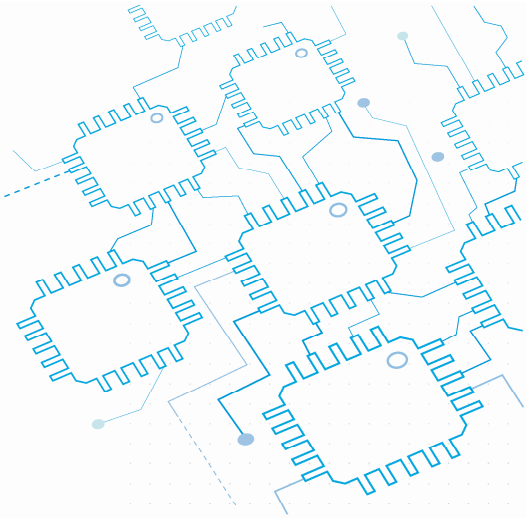
- Design clock = 50 MHz
- Reconfiguration latency
  - 344 ms – 211 kB
  - 346 ms – 212 kB

Conclusions



- The use of partial dynamic reconfiguration for effective implementation of the FIR filters
  - The internal ICAP reconfiguration interface reduces the reconfiguration time significantly.
  - Our experiments show the saved FPGA resources.

Acknowledgements



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